Reducing Energy Consumption in MCU-based Platforms with Low Design Margin Co-Processors

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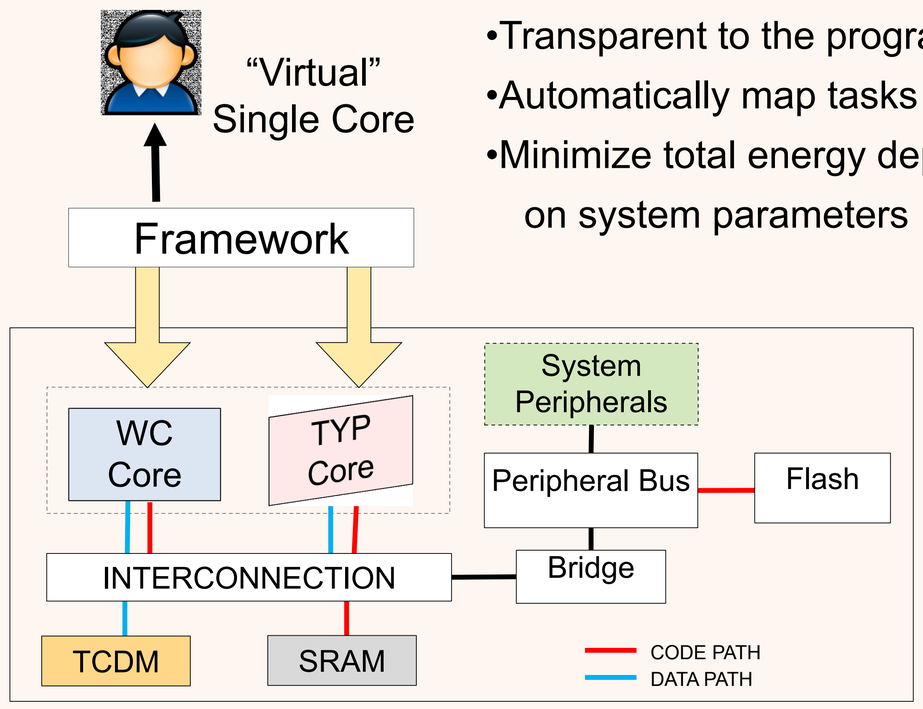
- Worst-Case (WC) Core manufactured with conservative margins has **low** energy efficiency
- Typical (TYP) Core manufactured with aggressive margins has a **high** energy efficiency
- Post-synthesis simulations show up to **30% efficiency boost**
  - TYP might run at a **reduced** frequency
  - WC core **needed** to guarantee minimum performance

Proposed Architecture:

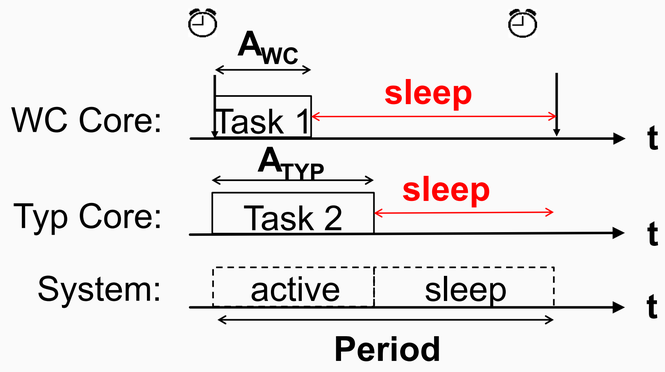
- Dual-core containing one **WC**, and one **TYP** core
- **Guaranteed** performance with possible **energy savings**



Framework requirements:

- Transparent to the programmer
- Automatically map tasks to cores
- Minimize total energy depending on system parameters

Sample Dual-Core (Parallel) Execution:

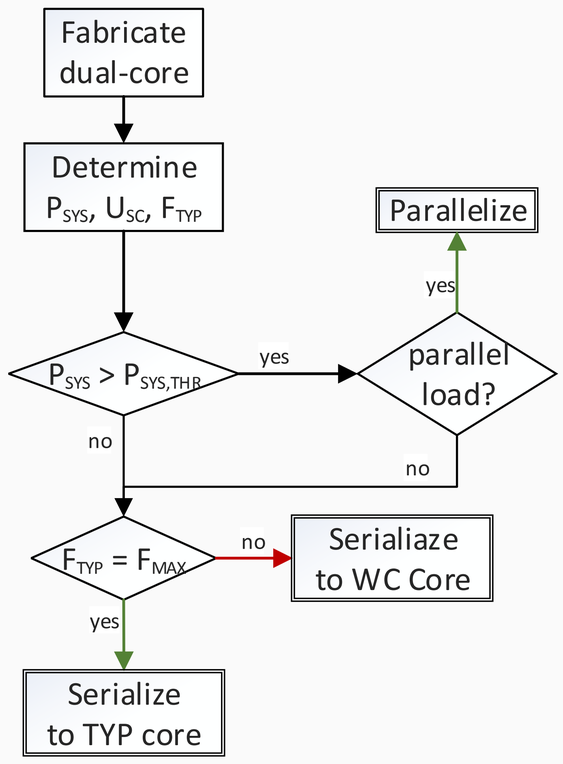


Power Model:

	Active	Sleep
WC	163.2 mW	9.6 mW
TYP	114.24 mW	6.74 mW

- P_{SYS} is an unknown constant.
- $P_{SYS} = P_{sleep,SYS}$ only when **both** cores in sleep

Dual-Core MCU Flow Chart:



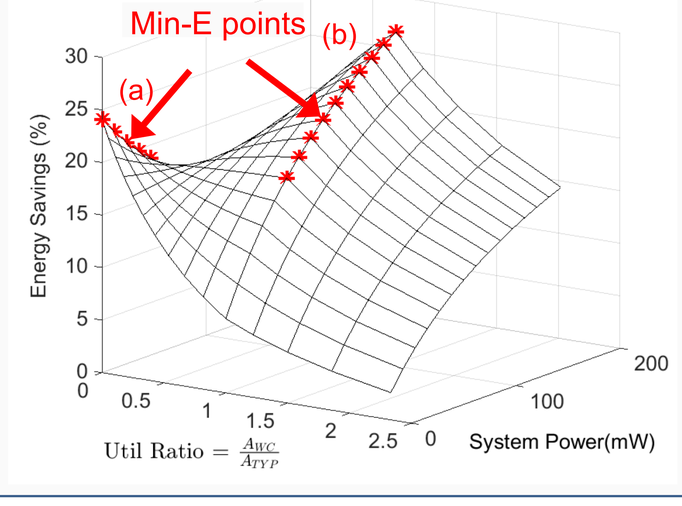
Optimization problem:

$$\min E_{TOT,DC} \Longrightarrow \min A_D * (P_{\Delta,\mathrm{TYP}} - P_{\Delta,\mathrm{WC}} + P_{\Delta,\mathrm{SYS}})$$

$$A_D^* = \begin{cases} A_{TYP} + A_{WC} \text{ if } (P_{\Delta,\mathrm{TYP}} - P_{\Delta,\mathrm{WC}} + P_{\Delta,\mathrm{SYS}}) < 0 \\ 0 \text{ if } (P_{\Delta,\mathrm{TYP}} - P_{\Delta,\mathrm{WC}} + P_{\Delta,\mathrm{SYS}}) \geq 0 \end{cases}$$

↳ Optimal mapping depends on **power ratios**

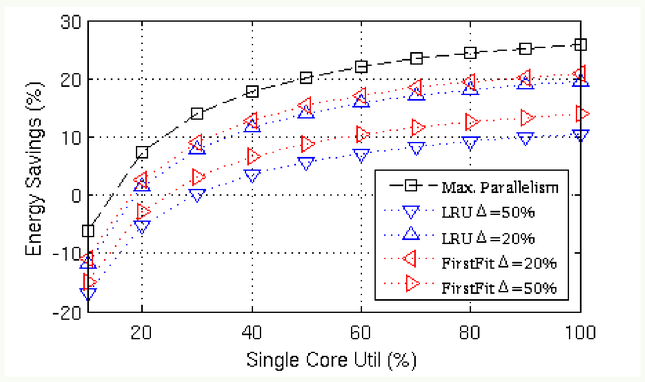
Design Space:

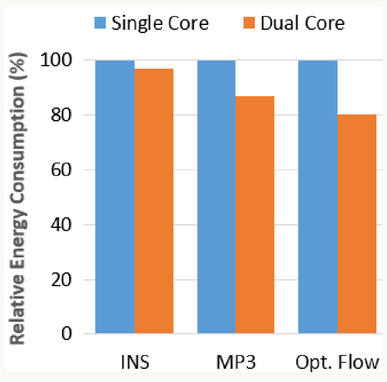


Experimental Results:

- Instruction Accurate (SystemC) simulation environment
- Synthetic + real world benchmarks show significant savings

Results calculated with: $P_{SYS} = P_{WC}$ and $F_{TYP} = F_{MAX}$

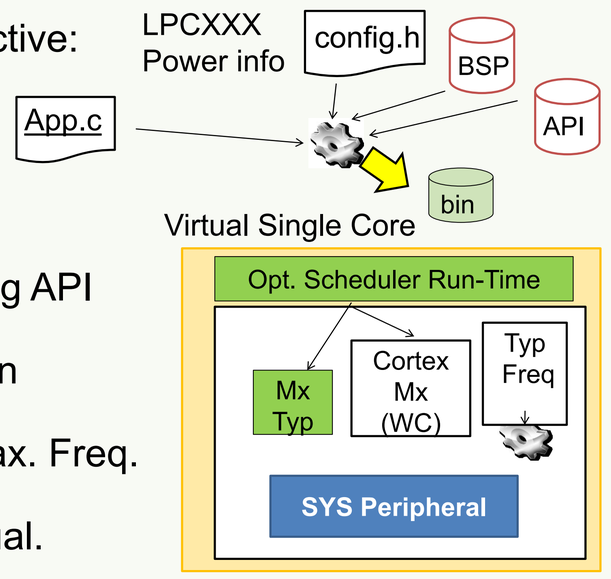




End Product:

From the developer's perspective:

- Select the platform.
  - Using config.h
- Port and compile APP, linking API
- At boot time – self-calibration
  - Determine TYP Core's max. Freq.
- Execute the program as usual.



References:

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