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- Worst-Case (WC) Core manufactured with conservative margins has low energy efficiency
- Typical (TYP) Core manufactured with aggressive margins has a high energy efficiency
- Post-synthesis simulations show up to 30% efficiency boost
- TYP might run at a reduced frequency
- WC core needed to guarantee minimum performance

Proposed Architecture:
- Dual-core containing one WC, and one TYP core
- Guaranteed performance with possible energy savings

Sample Dual-Core (Parallel) Execution:

<table>
<thead>
<tr>
<th>WC Core</th>
<th>TYP Core</th>
<th>System</th>
</tr>
</thead>
<tbody>
<tr>
<td>Task 1</td>
<td>Task 2</td>
<td>Active</td>
</tr>
<tr>
<td>sleep</td>
<td>sleep</td>
<td>WC Core</td>
</tr>
<tr>
<td>t</td>
<td>t</td>
<td>163.2 mW</td>
</tr>
<tr>
<td>AWC</td>
<td>ATYP</td>
<td>Sleep</td>
</tr>
<tr>
<td></td>
<td></td>
<td>TYP Core</td>
</tr>
<tr>
<td>sleep</td>
<td></td>
<td>114.24 mW</td>
</tr>
<tr>
<td>t</td>
<td></td>
<td>Parallelize</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Minimize total energy depending on system parameters</td>
</tr>
<tr>
<td>Period</td>
<td></td>
<td>System Parameters</td>
</tr>
</tbody>
</table>

Framework requirements:
- Transparent to the programmer
- Automatically map tasks to cores
- Minimize total energy depending on system parameters

Power Model:

<table>
<thead>
<tr>
<th></th>
<th>WC</th>
<th>TYP</th>
</tr>
</thead>
<tbody>
<tr>
<td>Active</td>
<td>163.2 mW</td>
<td>114.24 mW</td>
</tr>
<tr>
<td>Sleep</td>
<td>9.6 mW</td>
<td>6.74 mW</td>
</tr>
</tbody>
</table>

- \( P_{SYS} \) is an unknown constant
- \( P_{SYS} = P_{MIN\_SYS} \) only when both cores are in sleep

Design Space:

Optimization problem:

\[
\min E_{TOT,DC} \Rightarrow min A_D * (P_{\Delta TYP} - P_{\Delta WC} + P_{\Delta SYS})
\]

\[
A_D = \begin{cases} 
ATYP + AW&C & \text{if} (P_{\Delta TYP} - P_{\Delta WC} + P_{\Delta SYS}) < 0 \\
0 & \text{if} (P_{\Delta TYP} - P_{\Delta WC} + P_{\Delta SYS}) \geq 0 
\end{cases}
\]

Optimal mapping depends on power ratios

End Product:

From the developer’s perspective:
- Select the platform.
- Using config.h
- Port and compile APP, linking API
- At boot time – self-calibration
- Determine TYP Core’s max. Freq.
- Execute the program as usual.

Experimental Results:
- Instruction Accurate (SystemC) simulation environment
- Synthetic + real world benchmarks show significant savings

Results calculated with: \( P_{SYS} = P_{WC} \) and \( F_{TYP} = F_{MAX} \)

References: