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A Robust Sensing Platform for High Alpine Sensor Networks

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Abstract

This work documents the design of a *wireless sensor network* (WSN) platform for high alpine deployments. This new platform is intended to replace the current sensor nodes deployed by the PermaSense group, a research consortium devoted to developing and deploying WSNs in the high Alps. The new sensing platform is based on the *Dual-Processor Platform* (DPP) architecture. Meaning that application and communication tasks are mapped to different processors, interconnected via BOLT, an interprocessor communication mechanism that keeps power, clock and timing domains strictly decoupled. The new platform consists of two parts. Firstly, there is a communication module with a communication processor and BOLT chip. Secondly, there is a *sensor interface board* (SIB) with power management circuitry, sensor interface circuitry and an application processor. A prototype of the SIB has been developed in this thesis, and a communication module is currently in development. Initial tests show that the SIB is fully functional. Moreover, sleep current consumption shows an order of magnitude improvement over past PermaSense sensor platforms, and results for active current consumption are promising.

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Chapter 1

Introduction

The vision on *wireless sensor network*s (WSNs) has changed significantly over the past twenty years. Where Kahn et al. (1999) [1] presented a futuristic vision of cubic millimeter sized *smart dust*, modern work focuses on realistic, manufacturable designs. To this end, modern research is often supported by real world sensor deployments.

For example, the PermaSense [2] project studies practical WSN applications for harsh, high-mountain environments. In order to evaluate the real world performance of these WSNs, the PermaSense consortium operates a number of test networks in the Alps, one of which is shown in Figure 1.1. As these deployments have many common requirements, a standardized sensing platform was developed, and is used across different deployments.

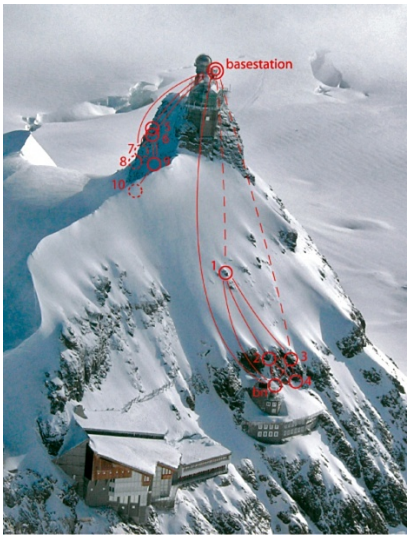
This platform is build around a Tinynode processing and radio module, that plugs in to a so called *sensor interface board* (SIB). The former is an off-the-shelf component, while the later is a custom designed *printed circuit board* (PCB). The SIB's function is to support the Tinynode, by providing it both power and an interface to a broad range of analog and digital sensors.

However, just as the WSN community has become wiser, so has the PermaSense team. The know-how gathered over the past years, together with the advance in technology has given rise to new sensor node requirements. Therefore, the time has come to develop a new sensing platform.

This new platform will be based on the *Dual-Processor Platform* (DPP) architecture [3]. The DPP architecture is a novel approach to WSN nodes, that imposes a strict separation between application (e.g. measurements) and communication (e.g. packet forwarding) tasks. It does so by mapping both types of tasks to different processors, and connecting them using BOLT [4]. BOLT is a interprocessor messaging mechanism that keeps the processor' power, clock and timing domains strictly separated.

Similarly to the current sensing platform, the new one will consists of a SIB that mates with a radio module. The new SIB will have similar functionality to the old SIB, but will also have an on board processor to run application tasks. The radio module will only be used for communication tasks, much similar to a network interface card in commodity computing products.

This thesis documents the design of this new SIB. The design of the radio module is a parallel effort.



(a) Locations of the sensor nodes. Circles indicate sensor nodes, lines show the network links between them.

(b) A typical sensor node installation.

Figure 1.1: A PermaSense WSN deployment.

Chapter 2

Background

2.1 PermaSense

The PermaSense [2] consortium consists of a group of interdisciplinary researchers from multiple Swiss research institutions and companies. The self stated goal of the consortium is to "develop, deploy and operate wireless sensing systems customized for long-term autonomous operation in high-mountain environments" [2].

Roughly speaking, PermaSense combines the interests of two groups: On the one hand, there are the electrical engineers. They are mainly interested in developing and deploying WSN infrastructure as a goal in itself. They ask questions like "How long does the sensor network stay operational?" or "How reliable is the data we gather?". On the other hand, there are the natural scientists that interpret the gathered data. They ask questions like "What trends are visible in the data?" or "What is the influence of global warming on permafrost[1]?". High-alpine sensor networks combine the interests of both groups: the electrical engineers see the harsh environment as an excellent benchmark for the robustness of the sensor electronics, and the natural scientists get access to datasets that would be infeasible to acquire in any other way.

This thesis is written from the perspective of the engineers. Namely, it discusses the design and prototyping of a new sensor system.

2.2 Wirless Sensor Networks

*Wireless sensor network*s (WSNs) are — as the name suggests — wireless networks that consists of multiple *sensor nodes*. These sensor nodes are typically small and low power devices with one or more sensors attached to them. They are often deployed in hard to access locations, and should therefore function as independently as possible. Furthermore they are typically battery powered, requiring the developer to treat power as a scarce resource. For example, the sensor nodes deployed by the PermaSense team require a minimum of three years of operation on a single D sized battery.

Because of these extreme power requirements, WSN nodes can not use regular wireless technology like IEEE 802.11 (or, in more human terminology: "WiFi"). Instead they follow standards specifically designed for low power operation, most notably IEEE 802.15.4 (unfortunatly, no human compatible name is available for this standard, but it forms the basis for the ZigBee [5] specification).

[1] *Permafrost* is permanently frozen ground.

In order to span large distances using these low power radios, WSNs typically operate as a mesh network. Data packets are forwarded over this network towards a special node called the *sink* or *base station*. The sink logs this data to permanent storage, forwards the data over the internet (e.g. via a cellular connection), or does both. Because of the higher power requirements for the sink (mass storage devices or cellular radios are typically power hungry), they are usually installed in a location with grid power access, or outfitted with solar cells. A typical WSN topology is shown in Figure 2.1.

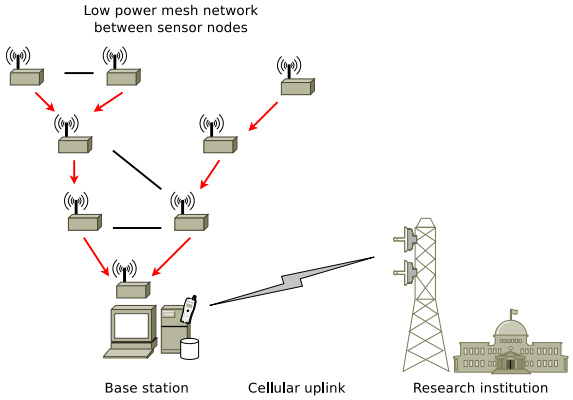


Figure 2.1: Schematic diagram of a typical WSN setup. The sensor nodes form a mesh network and forward data packets towards the base station. The base station writes the data to disk and forwards it over the cellular network to the research institution. Lines between sensor nodes show the links in the mesh networks. The red arrows show the paths that packets travel over.

2.3 Sensor Interface Board

The current sensor networks deployed by the PermaSense team are based on the Shockfish Tinynode [6]. As the Tinynode is only a processing and communications module, it must be supported by additional hardware before it becomes a fully functional sensor node. Therefore, the PermaSense team has developed the sensor interface board.

The *sensor interface board* (SIB) is a custom build PCB containing all the circuitry needed to support the Tinynode. The most important components of the SIB are:

- Circuitry to interface the Tinynode with a wide range of analog and digital sensors.
- A D sized battery to power the sensor node.
- Power regulation circuitry to generate a number of (switchable) voltage rails.
- Sensors to monitor the node's health: a temperature sensor, a humidity sensor and power monitors.
- User interface circuitry: LEDs, a reset button, a buzzer, ...

There are currently two generations of the SIB. Figure 2.2 shows how a sensor node based on the first generation SIB (also known as SIB1) looks like. The second generation SIB (SIB2) is an incremental update to the first one. The main difference is that it is designed for a larger metal housing.

This thesis documents the design of a third generation SIB (SIB3), designed to replace the tinynode with the *Dual-Processor Platform* (DPP).

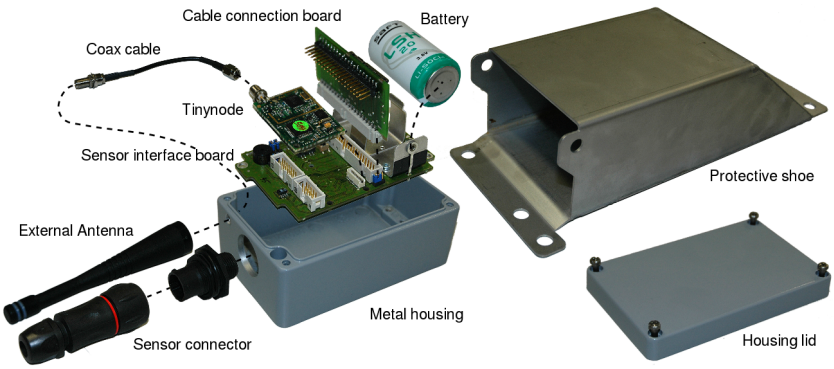


Figure 2.2: Exploded view of a PermaSense sensor node based on the first generation *sensor interface board* (SIB).

2.4 Dual-Processor Platform

In the first two generations of the SIB, a Tinynode is used as a processing and communication module. Because a single microcontroller is used for both communication (e.g. forwarding packets from other nodes) and application tasks (e.g. performing measurements), resource interference between these two tasks is possible and even likely. As such interference can have a negative impact on performance, it is undesirable.

The *Dual-Processor Platform* (DPP) [3] is a wireless sensor node architecture that decouples the communication and application domain by running the tasks for each of them on a dedicated processor. These two processors — called the communcation and application processor — are then connected to each other using BOLT [4]. BOLT is a processor interconnection mechanism that allows two processors to exchange messages in a fully asynchronous manner, while fully decoupling the time, power and clock domains. It does so by placing an active component, a *message buffer* between the communicating processors, and allowing them to read and write from this buffer according to their own schedule. We will refer to this active component as the *BOLT chip*.

Another advantage of the DPP architecture is that it allows for a modular design, where components can easily be exchanged. This is mainly thanks to the truly modular nature of a BOLT based interconnect. Figure 2.3 shows one of the early prototypes of the DPP architecture. The pluggable design of the BOLT module is a powerful demonstration of the modularity of the DPP design.

The third generation SIB will be based on the DPP architecture. The application processor will be embedded onto the SIB, and a BOLT compatible interface to connect to a communication module will be provide.

2.5 Ultra-Low Power Electronics Design

WSN deployments typically last for extensive periods of time. Because the nodes are usually battery powered, energy must be treated as an extremely scarce resource when designing a sensor node. Common techniques for ultra-low power electronics design are:

Using low power components When selecting components, care must be taken to select components with low active and quiescent current draws. For example, the popular `LD1117V28` 2.8 V linear voltage regulator [7] has a maximum quiescent current draw of

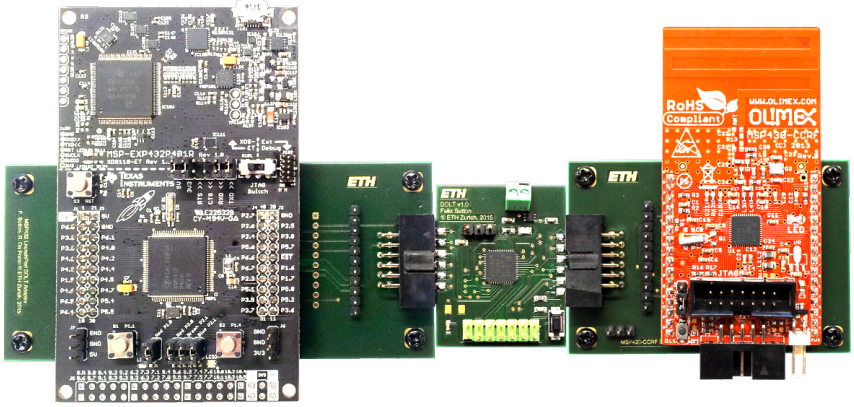


Figure 2.3: One of the early prototypes of the *Dual-Processor Platform* (DPP). A BOLT module (center) connects a `MSP432` application processor (left) with a `CC430` communication processor (right).

10 mA. At the same time, the `TPS78228` regulator [8], designed for ultra-lower power operation, has a quiescent current draw of at most 1.4 µA. A difference of four orders of magnitude!

Duty cycling Most active electronic components have high current consumptions, even when they are just idle. For example, when the `MSP432` microcontroller [9] is in `running` mode, it can easily consume a couple of mA, even when it is not doing any useful work. As most applications do not need all their resources all of the time, large energy savings can be accomplished by placing individual components in sleep mode. To come back to the example, when placed in its deepest sleep mode, the `MSP432` consumes only 25 nA.

Power gating As not all electronic components have ultra-low power sleep modes, or to even further reduce power consumption, it can be useful to completely disable a power rail. Let us consider a power rail generated by the `TPS78228` regulator discussed earlier. When the `TPS78228` is placed in shutdown mode, no more power is supplied to its output pin. Thus, the power draw of the components it powers is completely eliminated. Furthermore, when placed in shutdown mode, the `TPS78228` consumes merely 130 nA. Note however, that care must be taken that no power "leaks" into the disabled components, for example through an active signal line.

In the third generation SIB design, all of these techniques will be extensively used.

Chapter 3

Design

3.1 General Considerations

Past generations of PermaSense sensor nodes have all been based on a Tinynode that plugs in to a *sensor interface board* (SIB). Even though the new design will not be based on the Tinynode anymore, it will still consist of a SIB that connects to a communication module. This is discussed in more detail in Section 3.3. During this thesis, only the new SIB will be developed. The design of the new communication module is a parallel effort, that — at the time of this writing — has not been completed yet.

As the second generation *sensor interface board* (SIB) is a proven design, it was decided to use it as the basis for the design of the third generation SIB. However, the new SIB will be based on the *Dual-Processor Platform* (DPP) architecture, rather than to be build around a Tinynode. Based on good experiences in our research group, an `MSP432` will be used as application processor.

Using this more modern processor allows for a significant design simplification. The reason for this is twofold. Firstly, the limited pin count of the Tinynode required many signals to share the same physical connections. Because of this, complex demultiplexing circuitry was required on the SIB. As the `MSP432` has a plethora of pins, this will not be necessary any more. Secondly, because the `MSP432` has a large amount of on board peripherals, many of the components on the second generation SIB (e.g. external *universal asynchronous receiver/transmitter*s (UARTs)) can be eliminated.

The design of a new SIB is also an opportunity for design *clarification*. Through years of iterative design by multiple people, the documentation for the second generation SIB has lost some of its consistency and transparency. One of the goals of the new SIB design is to bring these back. Therefore, a strong focus is placed on creating clean schematics, clear code, consistent naming and a well documented design process throughout the project.

3.2 Requirements

At the beginning of this thesis project, a number of requirements for the new SIB were formulated. The most important ones are listed bellow. For a full overview, the reader is referred to the specification document referenced in Appendix C.

1. The SIB should be based on the Dual-Processor Platform architecture.
2. The SIB should be designed for the `MSP432` processor.

3. The SIB should be capable of long-term storage.
4. It should be possible to reset the SIB when the sensor node box is sealed.
5. The SIB should provide four differential *analog-to-digital converter* (ADC) channels with variable gain.
6. The SIB should provide two single ended ADC channels with variable gain.
7. The SIB should be able to interface digital sensors over SDI-12 [10], RS-232 and optionally RS-485.
8. The SIB should have 6 digital outputs.
9. The SIB should have two switched 12 V outputs.
10. An input for an external 12 VDC supply should be available. This supply is most likely to be a solar powered 12 V battery system. The SIB should be able to internally generate a 12 V rail when no external 12 V supply is available.
11. The SIB should be powered by a D sized Li-$SOCl_2$ battery.
12. The SIB should be able to monitor its own health. That is, it should be able to monitor:
    (a) Its input voltages and battery current consumption.
    (b) Its internal temperature and humidity.
13. The new sensor platform should be usable as a drop in replacement for current PermaSense deployments.

It should be noted that these are all *soft* requirements. If for some reason a requirement turns out to be unfeasible, or if deviating from it would significantly enhance the new platform, the requirements can be changed.

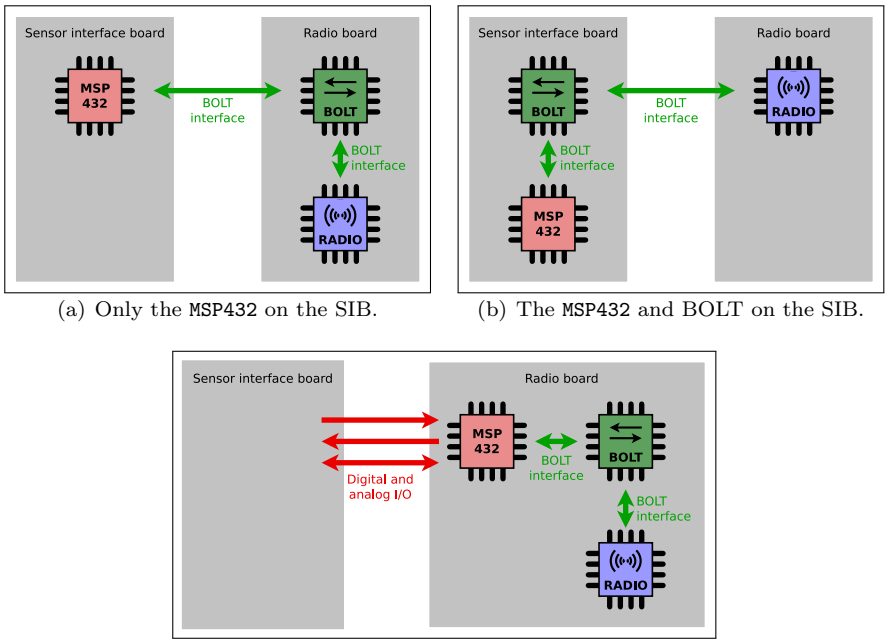
3.3 Architecture Selection

As stated in Requirement 1, the new SIB should be based on the DPP architecture. This means that the design must consists of an application processor (the `MSP432` per Requirement 2), a communication processor (or *radio*) and a BOLT module. Because a three board design (as in Figure 2.3) is cumbersome from a mechanical perspective, it was decided to place two or more of these components on the same board.

Furthermore, in order to keep the design compatible with future radio modules, and to make it possible for the radio module to be used by multiple projects, it was decided not to place the radio circuitry on the SIB. Rather, a radio daughter board will plug in to the SIB, similar to how the Tinynode plugs in to the second generation SIB. This gives rise to the question, "Which components should be placed on the radio module, and which ones on the SIB?". Three possible answers, shown in Figure 3.1, were considered.

Architecture A (Figure 3.1(a)) places only the `MSP432` on the SIB, and places both the BOLT and radio chip on the radio board. This has the advantage that the `MSP432` can be closely integrated with the SIB, and that the interface between the two boards is simple. Furthermore, the radio board can be developed independently from the SIB.

Architecture B (Figure 3.1(b)) is very similar to architecture A, but places the BOLT chip on the SIB rather than on the radio board. Which one of these two architectures is better, is a rather philosophical question. Should BOLT be primarily seen as a feature of the radio, or of the application processor?



(a) Only the `MSP432` on the SIB.

(b) The `MSP432` and BOLT on the SIB.

(c) Everything on the radio board.

Figure 3.1: Schematic representations of possible implementations of the DPP architecture.

Architecture C (Figure 3.1(c)) places all three components on the radio board. This architecture is the closest to the approach of the first and second generation SIB: no processing or communication is done on the SIB. Close integration with the `MSP432` is still possible, but would require a complex interface between the two boards. Alternatively, multiple logical connections could be multiplexed over a simpler physical interface.

Considering the above, it was chosen to use Architecture A. There are three main reasons for this. Firstly, placing the `MSP432` on the sensor interface board is preferable because it simplifies close integration of the microcontroller with the SIB. Secondly, Assuming that a standardized logical interface between the application processor (`MSP432`) and communication processor (radio) is defined, Architecture A allows the user to exchange the radio board (possible with one from another project), without having to reprogram the radio board or the SIB. Finally, it seems intuitively more natural to place the BOLT chip on the radio board. Facilitating asynchronous message passing is *not* one of the core features of the SIB. Rather, it should be seen as a feature provided by the radio board. Furthermore, as BOLT is still in active development, placing the BOLT chip on the radio board makes it easier to experiment with alternative versions.

3.4 Design Overview

The high level design for the new SIB is inspired by the design of the second generation board. However, there are some major differences between the old and new design. Probably the most significant of those is that the new SIB has an on board microcontroller, whereas the old design did not.

The two most important documents to understand the SIB3 design, are the *functional diagram* (Figure 3.2) and the *power diagram* (Figure 3.4).

3.4.1 The Functional Diagram

The functional diagram in Figure 3.2 shows that the MSP432 microcontroller is truly at the center of the design. The other major functional blocks in the design are:

The Radio Board is a daughter board of the SIB. As discussed in Section 3.3, it contains a BOLT chip and a radio module.

The AD7708 ADC is the main ADC used to digitize analog sensors. Being a Δ–Σ ADC, it has a lower sample rate than the MSP432 build-in *successive approximation* (SAR) ADC, but it offers a higher resolution (16-bit vs 14-bit) and has a programmable gain front end, partially fulfilling Requirements 5 and 6. The AD7708 has ten single ended inputs, that can be paired up to form differential inputs as needed. This fulfils Requirements 5 and 6 completely. A jumper allows the user to connect the analog ground for single ended measurements to digital ground, or to leave it floating. In the previous SIB design the same ADC was used. But because it was configured differently, and because it was also used to digitize signals internal to the sensor node, only six single ended channels were available to the user.

The SDCARD slot can be used to interface any microSD card in *Serial Peripheral Interface* (SPI) mode. This fulfils Requirement 3.

The Sensirion SHT31 provides temperature and humidity measurements of the inside of the sensor node. This fulfils Requirement 12b.

The Internal Serial Nr. is a silicon serial number allowing a SIB to be uniquely identified. The 1-Wire based DS2401 is used, because previous SIBs and some of the PermaSense sensors use the same chip. Thus, in order to satisfy Requirement 13, the new SIB must also support 1-Wire.

The Power Manager is not a physical component, but a logical one. It represents the SIB's ability to disable power rails as needed. It will be discussed in more detail in Section 3.4.2.

The Power Monitors allow the SIB to measure the battery voltage, battery current, and 12 V input voltage. They are digitized using the MSP432's internal ADC, leaving all channels of the AD7708 available to the user. This fulfils Requirement 12a.

The LEDs, Reset and Buzzer circuitry provides information to the user, and allows the user to reset the SIB. Because of their high current draw, the LEDs should *not* be used during deployment. Therefore, a hardware jumper to break the current path through the LEDs is included in the design. In order to meet Requirement 4, there is not only a reset *button* on the board, but their is also a reed switch connected to the reset pin of the MSP432. This allows the user to reset the board by holding a magnet close to the reed switch. Even when the SIB is in a sealed enclosure. The buzzer can be used to signal something to the user (e.g. a reset), even when the sensor node box is sealed.

The MAX3471, MAX3221 and 7400 Logic are used to generate RS-485, RS-232 and SDI-12 [10] compatible voltage levels, respectively. As no off-the-shelf components exists to generate SDI-12 compatible voltage levels, 7400 logic has to be used. These serial lines are used to communicate with digital sensors, as required by Requirement 7.

The UC_GPIO signals consist of seven signal lines directly connected to the MSP432, providing *general-purpose input/output* (GPIO) to the user, and fulfilling Requirement 8. Furthermore, all of these GPIOs can be used as inputs to the MSP432's internal 14-bit SAR ADC. Providing the user with up to seventeen ADC channels in total.

ESD protection is applied to all signal lines that leave the sensor node, and that will be used during deployment.

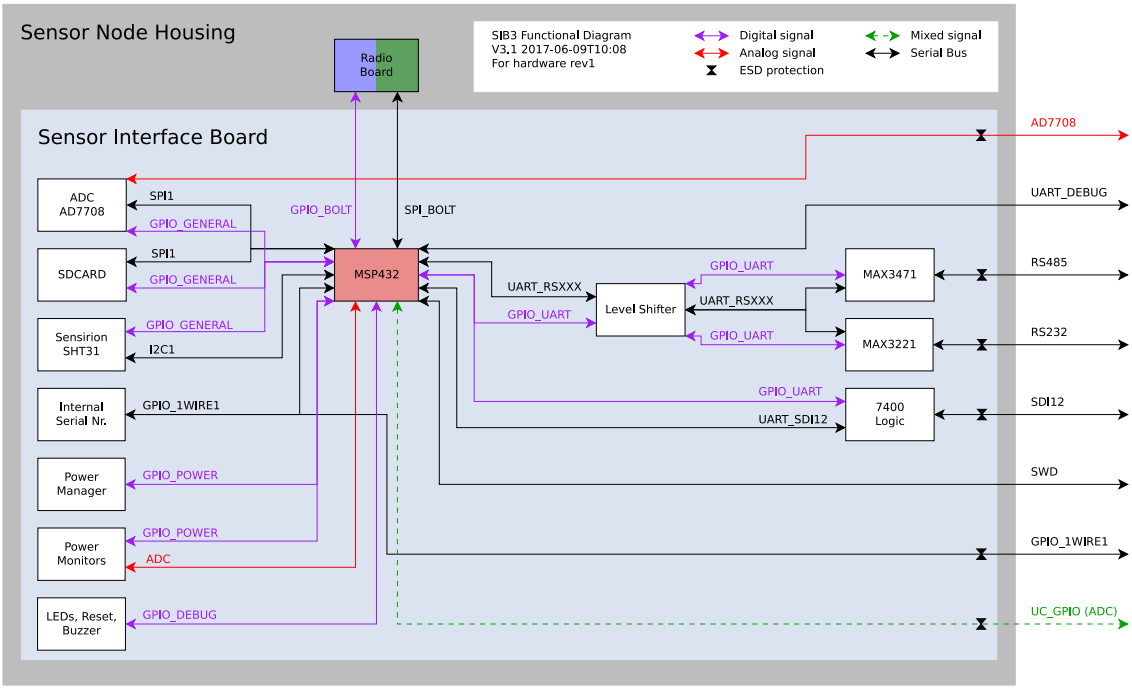


Figure 3.2: Functional diagram for the third generation SIB design. The naming in this diagram is followed throughout all design documents.

3.4.2 The Power Diagram

The power diagram in Figure 3.4 shows all voltage rails present on the SIB, and how they are generated.

Power enters the SIB at two points: via the battery, and via the 12 VDC input. Because of Requirement 11, the battery is a Li-$SOCl_2$ cell. The Saft `LSH 20` will be used, as this battery has performed excellently with the SIB2. It has a rated output voltage `VBAT` from 3.7 V to 3.2 V [11]. However, in practise, the voltage drops of quickly once a value of about 3.4 V is reached, as can be seen in Figure 3.3. Both the battery voltage `VBAT` and battery current `IBAT` can be monitored by the `MSP432`. From the battery voltage, the following supply rails are generated:

2V8 is the always-on supply rail that feeds the `MSP432`.

2V8_SW is the preferred voltage rail for components that the `MSP432` should be able to power gate. However, not all components support supply voltages as low as 2.8 V, thus additional power rails are required.

VBAT_SW is at the same voltage level as the `VBAT` rail, but can be disabled by the `MSP432`.

VSENSE is generated by a variable *low-dropout* (LDO) regulator. It is an extra supply voltage for external sensors, and is needed because some of the older PermaSense sensors operate on an input voltage of 3.2 V. It can be disabled by the `MSP432`. Optionally the `VSENSE` rail can be joined with the `2V8_SW` rail.

2V5_REF is the reference voltage for analog measurements. It is connected to the `AD7708`'s external reference input, and can be disabled by the `MSP432`.

12V_GEN is the internally generated 12 V rail, as required by Requirement 10. It can be used to power SDI-12 equipment when no external 12 V rail is available. It can be enabled by the `MSP432`.

The user should select whether he wants to use the external 12 V input (`12V_IN`) or the internally generated 12 V rail (`12V_GEN`) before deployment by setting a jumper. This prevents power hungry equipment from accidentally draining the internal battery.

From the selected 12 V rail — referenced as `12V_OUT` —, the `5V0` rail is generated. This rail is used to drive the signal line of the SDI-12 bus [10]. It should be noted that generating the `5V0` rail from the internally generated `12V_GEN` rail is power inefficient. However, the `5V0` rail is only used to drive the SDI-12 data line. According to the SDI-12 specification [10], this data line has a ground resistance of at least 80 kΩ[1]. This results in a maximal current draw of:

$$I = \frac{5V}{80k\Omega} < 64\mu A$$

Which is small enough that even low conversion efficiencies are tolerable.

The `12V_OUT` rail is also used to generate two switched 12 V outputs: `12V_SW1` and `12V_SW2`, as required by Requirement 9.

Appendix A provides an overview of what power rails should be active for which subsystems to be functional.

3.5 Board Input and Output

The SIB3 has a number of input and outputs, the most important of which will be discussed in this section.

[1] Assuming two devices are present on the bus.

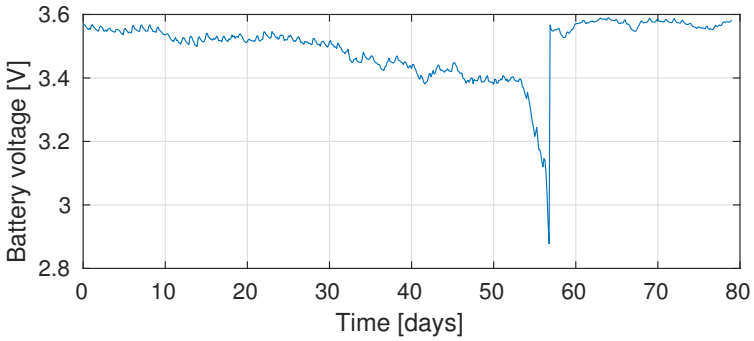


Figure 3.3: Plot showing how the battery voltage of a sensor node deployed on the Matterhorn evolves over time. It can be seen that once the battery voltage reaches 3.4 V, it drops of rapidly. Around the 57 day mark the battery is replaced. Other sensor nodes show the same behaviour. The zero point on the time axis does not correspond to the start of the deployment.

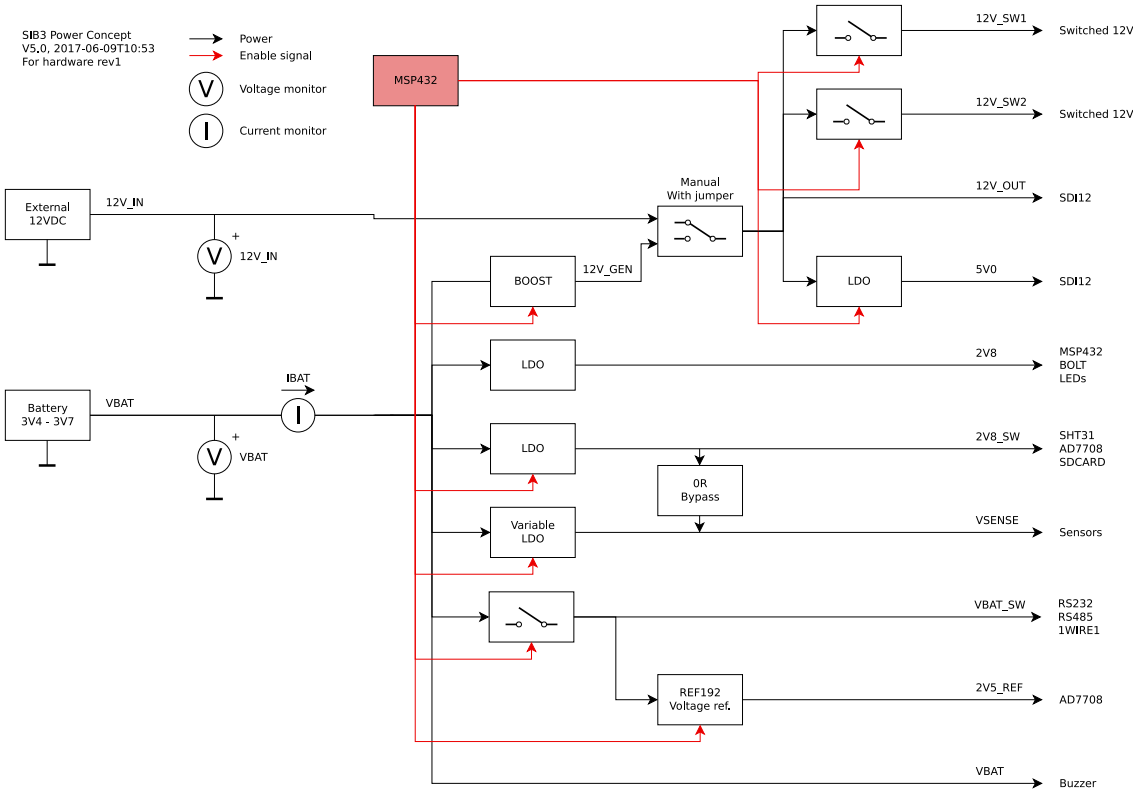


Figure 3.4: Power diagram for the third generation SIB design. The naming in this diagram is followed throughout all design documents.

3.5.1 Power Input

The SIB3 has four possible power inputs. Firstly, there is the battery, which is intended as the main power source during deployment. The board has a D sized battery holder, and guaranties support for input voltages in the 3.4 V to 3.7 V range. The battery is protected by a 500 mA self resetting fuse, and has no reverse polarity protection.

Secondly, there is the `VBAT` header next to the battery holder. This header is connected to the same power rail as the battery, and is intended to power the board while being serviced. There is no input protection present on this header, but a placeholder footprint for a fuse or series diode is provided.

Thirdly, there is the `VBAT` pin on the 40-pin sensor connector (see Section 3.5.2). While this pin is primarily intended as a power *output*, it can also be used as an input. When the SIB is powered through this pin, the power switch is not functional. This pin has *electrostatic discharge* (ESD) protection, but no fuse or reverse polarity protection.

Finally, there is the `12V_IN` pin on the 40-pin sensor connector (see Section 3.5.2). It can be used as a 12 V input (alternatively, the SIB can generate a 12 V rail internally). Support for voltages in the 9.6 V to 16 V range is guaranteed. This input is protected by a slow acting 2 A fuse, and has ESD protection.

3.5.2 Sensor Connector

The largest connector on the SIB3 is the 40-pin sensor connector. Its pinout is shown in Table 3.1. All power rails, the serial buses intended to communicate with external sensors, the ADC channels and the user GPIO (`UC_GPIO`) are all available on this connector. All of the pins are ESD protected.

Because of the series resistors in the ESD protection circuit, the current through the `12V_IN`, `12V_OUT`, `12V_SW1` and `12V_SW2` pins should not exceed 0.5 A continuously or 2 A at a 10 % duty cycle. The current through any of the other power rail pins should not exceed 100 mA. All these values are expressed per pin.

Pins from this connector are intended to be wired to a ruggedized and waterproof connector on the outside of the sensor note housing (i.e. the “Sensor connector” in Figure 2.2).

3.5.3 BOLT Connector

The BOLT connector is intended to connect the SIB to the radio module. However, as the design of this module is not yet know, and because a physical standard for the BOLT connector is still a work in progress, the first prototype of the SIB3 is designed to connect to the BOLT prototype shown in Figure 2.3. For a next tapeout of the design, the connector should be replaced. The current design provides ample of board space to place this new connector.

The pinout for the current BOLT connector is shown in Table 3.2. The connector provides the always on `2V8` rail, as BOLT modules are supposed to handle their own power management.

3.5.4 Debug UART Header

As its name suggests, the debug UART header can be used to connect to the debug UART. The UART header has a ground, `Tx`, `Rx` and reset pin. This last pin can be used to reset the microcontroller when a UART bootloader is used.

Table 3.1: Pinout of the 40-pin sensor connector

Pin	Function	Pin	Function
1	SDI12_DATA	2	12V_IN
3	RS485_A	4	12V_OUT
5	RS485_B	6	12V_SW1
7	RS232_RX	8	12V_SW2
9	RS232_TX	10	5V0
11	AD7708_CH7	12	GND
13	AD7708_CH8	14	2V5_REF
15	AD7708_CH1	16	GND
17	AD7708_CH2	18	VSENSE
19	AD7708_CH3	20	VBAT
21	AD7708_CH4	22	2V8_SW
23	AD7708_COM	24	2V8
25	AD7708_CH5	26	VBAT_SW
27	AD7708_CH10	28	GND
29	AD7708_CH9	30	GND
31	AD7708_CH6	32	GND
33	1WIRE1	34	UC_GPIO7
35	UC_GPIO6	36	UC_GPIO5
37	UC_GPIO4	38	UC_GPIO3
39	UC_GPIO2	40	UC_GPIO1

Table 3.2: Pinout of the BOLT connector

Pin	Function	Pin	Function
1	2V8	2	GND
3	BOLT_FUTURE_USE	4	BOLT_C_IND
5	BOLT_ACK	6	BOLT_TIM_REQ
7	BOLT_REQ	8	SPI_BOLT_SCLK
9	BOLT_MODE	10	SPI_BOLT_MISO
11	BOLT_IND	12	SPI_BOLT_MOSI

Chapter 4

Prototype

In order to verify the new SIB design, parts for five boards were ordered. These boards are a four layer design, and the schematic and PCB overlay can be found in Appendix D. One of these boards was assembled, and used to run a number of tests (see Section 4.1). The assembled prototype, can be seen in Figure 4.1. The results of these tests gave rise to a number of design changes that should be incorporated in a next iteration of the SIB3. These are listed in Section 4.2.

4.1 Testing

4.1.1 Test 1: Verification of Power Rails

Being faithful to the golden rule of electronics debugging ("they shall measure voltages"), the first test performed on the new SIB was a check of all voltage rails. For this test, all power rails were enabled by software, and the voltages on them measured.

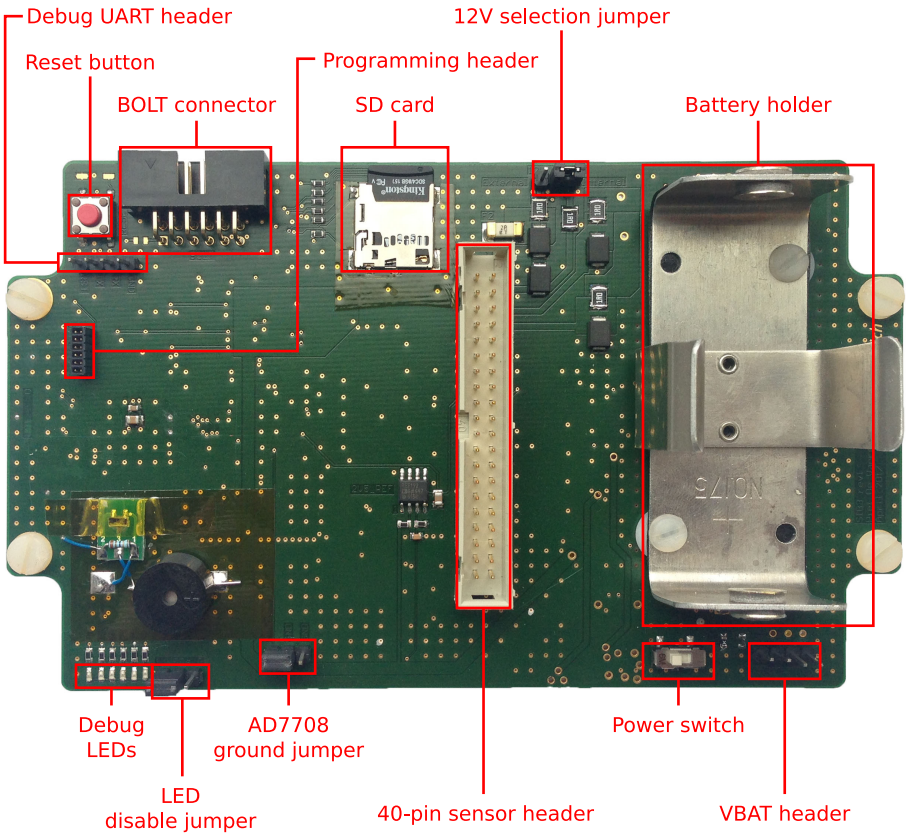
The results are shown in Table 4.1. All measured voltages are well within their specification. However, two measurements are noteworthy: the values of the `2V5_REF` and the `12V_GEN` rail.

The `2V5_REF` rail has a deviation of $-0.003\,\mathrm{V}$ from the design value of $2.500\,\mathrm{V}$. On first sight, this appears as a large deviation for a voltage reference, but consulting the datasheet of the `REF192G` [12], shows that the initial accuracy is $2.490\,\mathrm{V}$ to $2.510\,\mathrm{V}$. Thus, the measured value is well within specification. If required, the `REF192G` can be replaced by the pin compatible `REF192E`, which has an initial accuracy of $2.498\,\mathrm{V}$ to $2.502\,\mathrm{V}$.

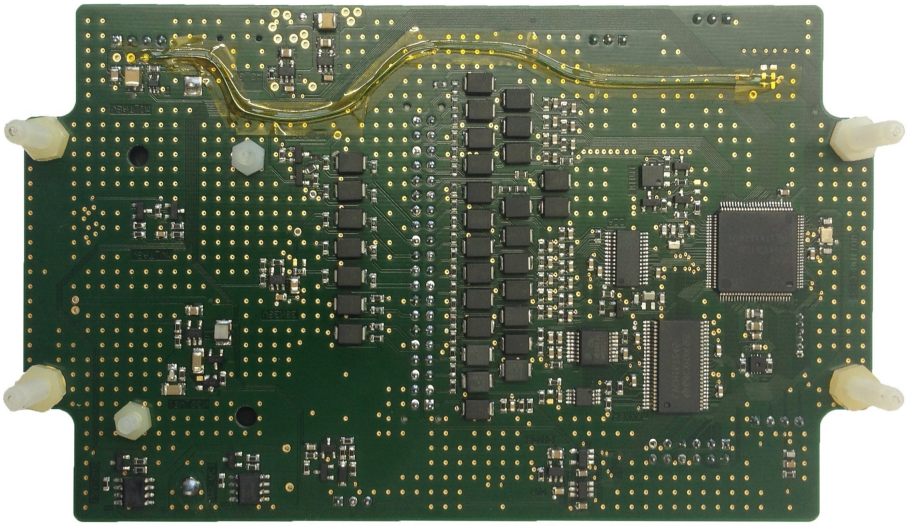
The `12V_GEN` rail measures at $11.53\,\mathrm{V}$, which is on the low side for an unloaded $12\,\mathrm{V}$ rail. However, the boost converter that generates the `12V_GEN` rail, is set to output $11.50\,\mathrm{V}$ by design. This value was copied from the SIB2 design. For a next iteration of the SIB3 design, this should be changed to $12\,\mathrm{V}$.

4.1.2 Test 2: Functional Verification

In order to functionally verify all parts of the design, a test application that interacts with all functional blocks was written. This code was written with the sole purpose of verifying the hardware design. It was *not* written to properly handle errors or to be power efficient, and should therefore *never* be used in anything that is even remotely close to production. However, the code can be used as guidance when writing a production grade application.



(a) Top side.



(b) Bottom side.

Figure 4.1: The first prototype of the third generation SIB.

The pseudocode for the test application is shown in Listing 4.1. All UARTs run at 115 200 baud, except for SDI-12, which runs at 1200 baud. The debug LEDs were used to display a counter keeping track of the program state. This counter was also written to the user GPIO pins (`UC_GPIO`). After some small hardware modifications (see Section 4.2), all subsystems where fully functional. The output from the debug UART is provided in Appendix B.

4.1.3 Test 3: Power Trace

In order to get a first impression of the new SIB's power consumption, a power trace of the test application from Section 4.1.2 was recorded. For this measurement the debug LEDs were disabled with a jumper. The test setup is shown in Figure 4.2. The SIB is connected to a bench power supply with a RocketLogger[1] [13] performing a series current measurement. Furthermore, the RocketLogger's digital inputs are connected to the `UC_GPIO` pins. This makes it possible to link the current measurements to the active program state.

The trace in Figure 4.3 shows that during operation, current consumption is relatively stable around 10 mA (the red dotted line). There are however, a number of clear increases in current draw:

When power is switched on there is a large current surge up to about 500 mA. This is because many capacitors on the board need to be charged. Because the system is not yet running when this peak occurs, it is not a problem for proper operation of the SIB. When the SIB's power source can not supply such a high current, the capacitors will charge slower, resulting in a wider but lower peak.

When the power rails are enabled there is another current peak, of about 160 mA. This peak is also caused by charging capacitors. The height of the peak can be reduced by switching on power rails in steps, instead of enabling them all at once.

When the buzzer is sound current rapidly varies from 20 mA to 35 mA.

When the SD card is accessed current peaks up to 60 mA are measured.

When the RS-232 transmitter is enabled current rises to about 35 mA.

This shows that the most power hungry components are the buzzer, SD card and RS-232 transceiver. Thus, when developing an application for the SIB, extra care must be taken to minimize their active times.

The trace also shows that when all switchable power rails are disabled, the current draw drops to approximately 5 mA (the green dotted line). This is the current drawn by the microcontroller when executing idle instructions. As the the microcontroller does not enter a low power state, this does *not* correspond to the standby current of the board. What this measurement *does* show us, is that enabling all power rails adds approximately 5 mA to the boards power consumption. This can be seen as a worst case increase, as in production grade applications, only the required voltage rails will be enabled.

4.1.4 Test 4: Deep Sleep Power Consumption

The test in Section 4.1.3 provides insight in the power consumption of the various board components when active. However, as the SIB will be heavily duty cycled during deployments, it is essential that the board has a low current consumption during (deep) sleep.

[1] The RocketLogger is an in house measurement device that can be used for precision, long term, voltage and current measurements. It also has digital inputs that can be sampled alongside the analog channels.

Table 4.1: Measured and design vaules of the power supply rails.

Rail	Design value	Measured value	Delta
VBAT	3.4 V to 3.7 V	3.595 V	+0.000 V
VBAT_SW	3.4 V to 3.7 V	3.591 V	+0.000 V
2V5_REF	2.500 V	2.497 V	−0.003 V
VSENSE	3.161 V	3.176 V	+0.015 V
2V8_SW	2.800 V	2.822 V	+0.022 V
2V8	2.800 V	2.812 V	+0.012 V
5V0	5.000 V	5.000 V	+0.000 V
12V_GEN	11.50 V	11.53 V	+0.03 V
12V_SW1	11.50 V	11.53 V	+0.03 V
12V_SW2	11.50 V	11.53 V	+0.03 V

Listing 4.1: Pseudocode for the functional verification program.

```
Main:
    Initialize all GPIO
    Initialize UART
    Initialize BOLT
    Sound buzzer for 1000 ms
    While True:
        Disable all power rails
        Wait 100 ms
        Read power monitors
        Enable all power rails
        Read power monitors
        Initialize SD card
        Read out SHT31 (on board temperature and humidity)
        Calibrate Channel 1 from the AD7708 (external ADC)
        Read out Channel 1 from the AD7708 (external ADC)
        Read out internal serial number over 1-Wire
        Send test string over RS-232
        Send test string over RS-485
        Send test string over SDI-12
        Send test string over BOLT
        Wait 500 ms

RS-232, RS-485 and SDI-12 interrupt routine:
    Read character from bus
    If character == '\n':
        Print out characters over debug UART
```

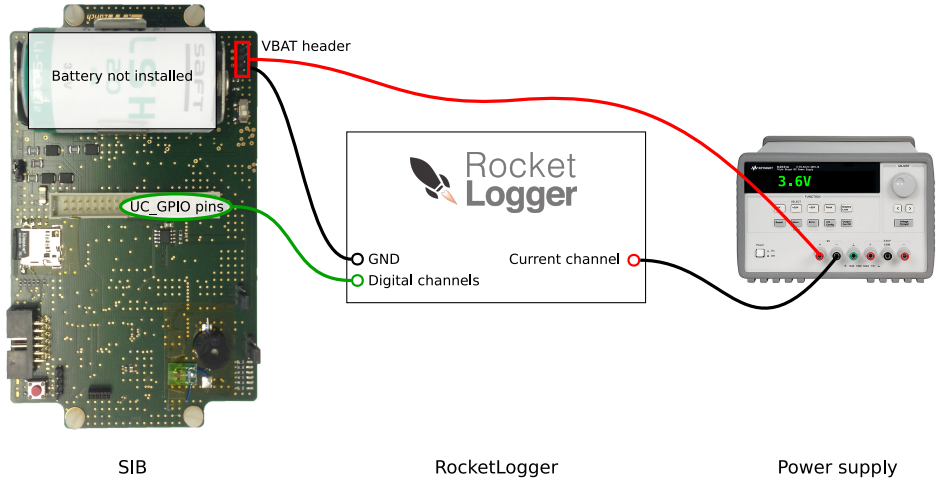


Figure 4.2: Test setup used to generate the power trace in Figure 4.3. A RocketLogger measures the current consumption of the SIB, and records the program state through the `UC_GPIO` pins.

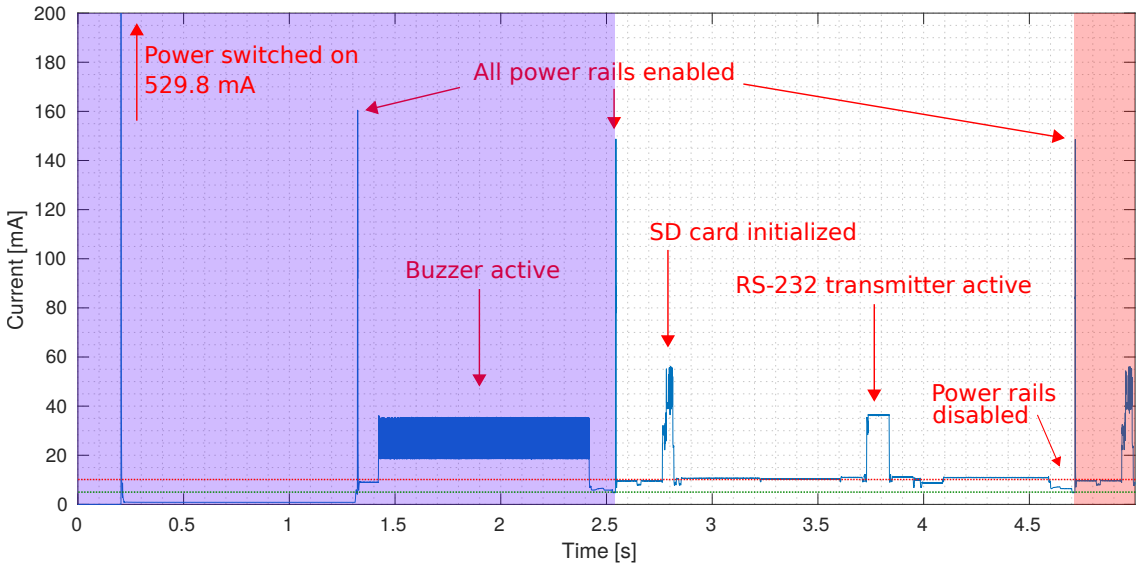


Figure 4.3: Power trace of the SIB3 functional test application in Listing 4.1. Three phases of the application are shown: initialization (purple), first iteration of loop (white) and the start of the second loop iteration (red). Power was supplied to the board from a bench top power supply, that was switched on around the 200 ms mark, as indicated in the figure.

It is therefore useful to quantify the minimal power consumption of the new SIB. That is, the current consumed by the board when it is placed in its lowest power mode. To that end, a test program that disables all power rails and places the MSP432 in its lowest power mode (LPM4.5) was uploaded to the board. Next all debugging equipment was disconnected, and the boards power consumption measured using a precision current meter. In order to better simulate deployment conditions, a sensor rod with four thermistors was attached. This setup is shown in Figure 4.4.

Once the microcontroller entered in to LPM4.5 mode, the board's power consumption dropped bellow 2 µA. Although this is a very promising result, it should be mentioned that the LPM4.5 mode will probably not be used during deployment, as the MSP432 can only be woken up from this mode by an external signal. We can however, use this measurement to predict the boards current consumption in other low power modes.

Two low power modes are likely to be used extensively in deployment applications: LPM3.5 and LPM0.

> **LPM3.5** is the lowest power mode still allowing wake ups from the MSP432's internal *real time clock* (RTC). Therefore, this mode is ideal to be used while waiting between measurement cycles. According to the MSP432's datasheet [9], the rated current consumption for this power mode is 630 nA.
>
> **LPM0** is the highest power sleep mode. It allows the microcontroller to be waken up by most of its internal peripherals. The rated current consumption for this power mode is 500 µA. This assumes a clock speed of 8 MHz and that all peripherals are inactive. Enabling a SPI module adds 40 µA to this value. Lowering the clock speed reduces these values further.

The MSP432's datasheet [9] states that the microcontroller's current consumption in LPM4.5 is 25 nA. Given that placing the MSP432 in LPM3.5 instead consumes about 600 nA more, and given the measurement value above, this suggests that the SIB3's current draw between measurement cycles will be well bellow 3 µA. For comparison, the SIB1 has a power consumption of 26 µA while sleeping [14]. No data for SIB2 is available.

During the functional test application from Section 4.1.2, almost all of the processors time is spend performing idle computation (i.e. time delay loops, flag polling or pin polling). In a production grade application this can be eliminated by configuring an interrupt and by placing the MSP432 in LPM0 until this interrupt fires. This means that the average current consumption of the MSP432 will effectively drop from the 5 mA measured in Section 4.1.3, to approximately 540 µA. It is also known from Section 4.1.2 that the the current consumption of all peripherals (except the buzzer, SD card and RS-232 transceiver) is upper bounded by 5 mA. Thus, the expected power consumption of the SIB3 during data acquisition can be upper bounded to $5\,\text{mA} + 540\,\mu\text{A} < 6\,\text{mA}$. It is important to remember that this is only an upper bound, and not the actual expected current consumption. The SIB1 consumes about 2 mA when performing its acquisition cycle (excluding RS-232 and ADC operation) [14].

4.1.5 Test 5: Sensor Rod Demo

This final test was designed to be as close as possible to a deployment situation. It is based on the functional test in Section 4.1.2, but with a number of modifications:

- The SIB is now battery powered, as this will be the power source used during deployment.
- A sensor rod is attached to the SIB. The sensor consists of a plastic rod with four metal rings, each thermally coupled to a thermistor. This type of sensor is used by the PermaSense team to measure temperatures at different depths beneath the surface. The schematic and wiring of the sensor are shown in Figure 4.5(b).

- Instead of digitizing one channel from the `AD7708`, all four channels connected to the sensor rod are digitized.
- The following information is periodically printed over BOLT:
  - The humidity and temperature measured with the `SHT31` sensor on the SIB.
  - The SIB's battery voltage and current.
  - The four temperatures measured by the sensor rod.

The full setup is shown in Figure 4.5. To verify proper functionality, the data transmitted over the debug UART and BOLT serial lines is monitored by a desktop computer. The BOLT output of this program is shown in Listing 4.2, the UART output in Appendix B. After the first iteration of the program loop, the `T1` metal ring was cooled down with freezer spray. It can be seen in the BOLT output (in Listing 4.2) that the measured temperature only decreases gradually. This is due to the large thermal mass of the metal rings on the sensor.

Listing 4.2: BOLT output of the sensor rod demo. Edited for readability.

```
1  Node Health (A): VBAT = 3.63 V  IBAT = 13.05 mA
2  Node Health (B): T = 24.51 deg. C    H = 45.89 RH
3  Sensor: T1: 24.14    T2: 24.22    T3: 24.19    T4: 24.18
4  ------------------------------------------------------
5  Node Health (A): VBAT = 3.63 V  IBAT = 15.36 mA
6  Node Health (B): T = 24.41 deg. C    H = 45.88 RH
7  Sensor: T1: 24.04    T2: 24.19    T3: 24.18    T4: 24.18
8  ------------------------------------------------------
9  Node Health (A): VBAT = 3.62 V  IBAT = 9.67 mA
10 Node Health (B): T = 24.09 deg. C    H = 45.62 RH
11 Sensor: T1: 15.27    T2: 23.52    T3: 24.14    T4: 24.17
12 ------------------------------------------------------
13 Node Health (A): VBAT = 3.62 V  IBAT = 9.58 mA
14 Node Health (B): T = 24.02 deg. C    H = 45.98 RH
15 Sensor: T1: 6.04    T2: 22.85    T3: 24.03    T4: 24.15
16 ------------------------------------------------------
17 Node Health (A): VBAT = 3.62 V  IBAT = 13.93 mA
18 Node Health (B): T = 24.14 deg. C    H = 46.92 RH
19 Sensor: T1: 0.70    CT2: 22.40    T3: 23.93    T4: 24.13
```

4.2 Design Modifications

Assembling and testing the first SIB3 prototype uncovered a number of changes that should be made to the SIB3 design. There are only two critical changes, which are listed bellow. A full list can be found in the design documents referenced in Appendix C.

- The vias under the SD card slot should be removed. They can cause short circuits with the contacts that mate up with the SD card. The SD card slot should be rotated 180 degrees.
- The buzzer should be replaced with the buzzer from the SIB2 design. It should be driven by a low side MOSFET.

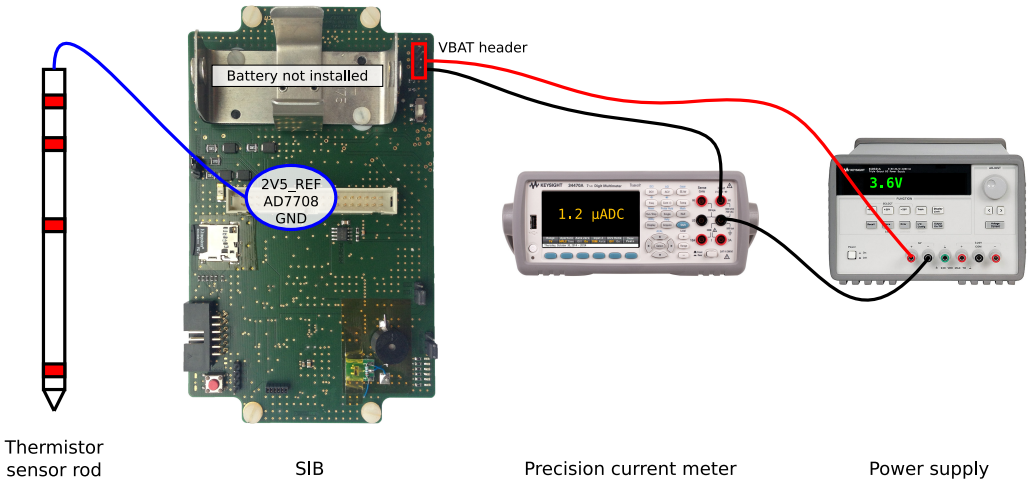
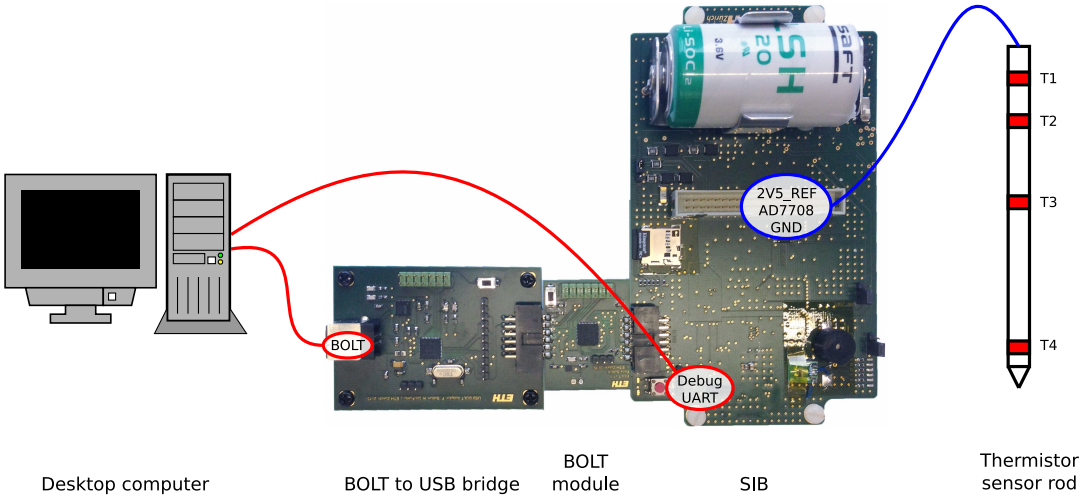
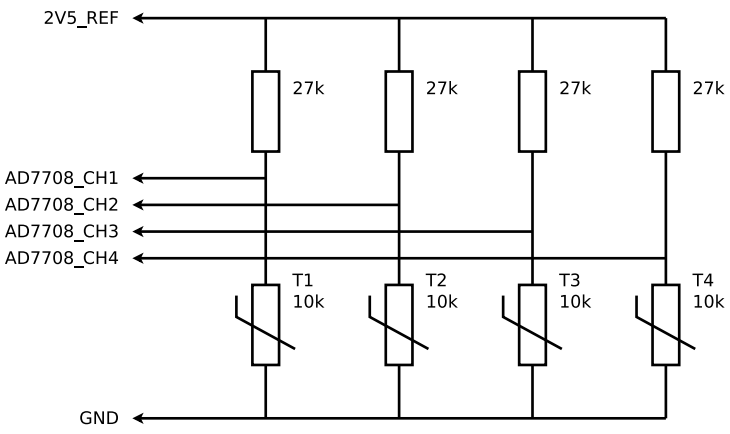


Figure 4.4: Test setup used to measure the deep sleep power consumption of the new SIB. The SIB is powered from a bench power supply, and its supply current is measured by a precision current meter. A thermistor sensor rod is attached to the 40-pin sensor header.



(a) A thermistor sensor rod is attached to a battery powered SIB. Debug UART and BOLT output is monitored with a desktop computer.



(b) Schematic and wiring of the thermistor sensor rod.

Figure 4.5: Test setup for the sensor rod demo.

Chapter 5

Conclusion and Future Work

The goal of this thesis was to design a robust sensing platform for high alpine wireless sensor networks. This design will serve to replace the current — outdated — platform used by the PermaSense consortium. However, as the current PermaSense platform is a proven design, it was used as a reference for the new one.

It was chosen to follow a similar approach as the current platform: a communication module plugs in to a *sensor interface board* (SIB). The later provides power and a sensor interface to the former. However, where in previous designs the communication module was also used for application tasks (e.g. reading out sensors), the new design follows the *Dual-Processor Platform* (DPP) architecture. The DPP architecture decouples communication and application tasks by mapping them to different processors, that communicate using BOLT. BOLT is a processor interconnect allowing asynchronous message passing while keeping the power, clock and time domains of the communicating processors strictly decoupled. More concretely, the new SIB includes a `MSP432` microcontroller that handles all application tasks. The communication module hosts the communication processor and the BOLT chip.

This design does not only limit resource interference between the communication and application domains, but it also allows closer integration between the application processor and the application itself. That is, by embedding the `MSP432` on to the SIB, it can be closely coupled in to the power management and sensor interface circuitry, resulting into an overall design simplification. Moreover, by keeping all application depended logic on the SIB, a single radio module design can be used across different projects.

A prototype SIB using this new architecture was designed, manufactured and tested. Initial tests show that the design is fully functional and shows excellent power performance. The new design improves sleep current consumption by an order of magnitude, and first measurements suggest that the active current consumption will at least match that of the old design.

The design of a communication module is a parallel effort that is still ongoing. Once it is completed, it can be combined with the SIB. Nevertheless, because the new sensing platforms follows the DPP architecture, the communication and application domains are fully decoupled. This means that code development for the new SIB does not have to wait for the completion of the communication module.

Bibliography

[1] J. M. Kahn, R. H. Katz, and K. S. J. Pister, "Next century challenges: Mobile networking for smart dust," in *Proceedings of the 5th Annual ACM/IEEE International Conference on Mobile Computing and Networking*, ser. MobiCom '99. New York, NY, USA: ACM, 1999, pp. 271–278. [Online]. Available: http://doi.acm.org/10.1145/313451.313558

[2] The PermaSense Consortium. (2016) The PermaSense Consortium. [Online]. Available: http://permasense.ch

[3] F. Sutton, R. D. Forno, D. Gschwend, T. Gsell, R. Lim, J. Beutel, and L. Thiele, "The design of a responsive and energy-efficient event-triggered wireless sensing system," in *Proceedings of the 14th International Conference on Embedded Wireless Systems and Networks (EWSN 2017)*. Uppsala, Sweden: ACM, Feb 2017, pp. 144–155.

[4] F. Sutton, M. Zimmerling, R. Da Forno, R. Lim, T. Gsell, G. Giannopoulou, F. Ferrari, J. Beutel, and L. Thiele, "Bolt: A stateful processor interconnect," in *Proceedings of the 13th ACM Conference on Embedded Networked Sensor Systems*, ser. SenSys '15. New York, NY, USA: ACM, 2015, pp. 267–280. [Online]. Available: http://doi.acm.org/10.1145/2809695.2809706

[5] ZigBee Standards Organization, *ZigBee Specifcation*, 2012.

[6] H. Dubois-Ferrière, L. Fabre, R. Meier, and P. Metrailler, "Tinynode: A comprehensive platform for wireless sensor network applications," in *Proceedings of the 5th International Conference on Information Processing in Sensor Networks*, ser. IPSN '06. New York, NY, USA: ACM, 2006, pp. 358–365. [Online]. Available: http://doi.acm.org/10.1145/1127777.1127831

[7] STMicroelectronics, *LD1117 Datasheet: Adjustable and fixed low drop positive voltage regulator*, 2013.

[8] Texas Instruments, *TPS78XX Datasheet: ultra-low quiescent current low-dropout linear regulator*, 2009.

[9] ——, *MSP432P401R Datasheet: SimpleLink Mixed-Signal Microcontrollers*, 2017.

[10] SDI-12 Support Group, *SDI-12 A Serial-Digital Interface Standard for Microprocessor-Based Sensors*, 2017.

[11] Saft, *LSH 20 Datahseet: Primary lithium battery*, 2006.

[12] Analog Devices, *REF19x Series Datasheet: Precision Micropower, Low Dropout Voltage References*, 2011.

[13] L. Sigrist, A. Gomez, R. Lim, S. Lippuner, M. Leubin, and L. Thiele, "Measurement and validation of energy harvesting iot devices," in *Proceedings of the 2017 Design, Automation & Test in Europe Conference & Exhibition (DATE 2017)*, Lausanne, Switzerland, Mar 2017.

[14] J. Beutel, S. Gruber, A. Hasler, R. Lim, A. Meier, C. Plessl, I. Talzi, L. Thiele, C. Tschudin, M. Woehrle, and M. Yuecel, "Permadaq: A scientific instrument for precision sensing and data recovery in environmental extremes," in *Proceedings of the 2009 International Conference on Information Processing in Sensor Networks*, ser. IPSN '09. Washington, DC, USA: IEEE Computer Society, 2009, pp. 265–276. [Online]. Available: http://dl.acm.org/citation.cfm?id=1602165.1602190

List of Acronyms

Acronyms

ADC analog-to-digital converter

DPP Dual-Processor Platform

ESD electrostatic discharge

GPIO general-purpose input/output

LDO low-dropout

LED light emitting diode

MOSFET metaloxidesemiconductor field-effect transistor

PCB printed circuit board

RTC real time clock

SAR successive approximation

SIB sensor interface board

SPI Serial Peripheral Interface

UART universal asynchronous receiver/transmitter

WSN wireless sensor network

Appendix A

Power Rail Dependencies

Table A.1 provides an overview of which power supply rails should be active when using a SIB3 subsystem.

Table A.1: Overview of (switchable) supply rail depenencies for SIB3 subystems.

Subsystem	**Supply Rail**
BOLT	None
AD7708	2V8_SW
SDCARD	2V8_SW
SHT31	2V8_SW
Internal Serial Nr.	2V8_SW VBAT_SW
LEDs	None
Buzzer	None
UART_DEBUG	None
RS485	2V8_SW VBAT_SW
RS232	2V8_SW VBAT_SW
SDI12	2V8_SW 12V_GEN[1][2] 5V0

[1] Unless 12 V is supplied through the 12V_IN rail.
[2] The right 12 V supply rail should be selected with a jumper.

Appendix B

Test UART Output

During the functional system test (Section 4.1.2) and sensor rod demo (Section 4.1.5) the messages on the debug UART were recorded. Bellow the output of a single loop cycle of the sensor rod demo program is given. The output of the functional system test is largely similar.

```
At the top of the test loop
     1110 main.c 64: POWER: Disabling all power rails
     2115 driver.c 864: VBAT: 3.639488 V
     2119 driver.c 865: IBAT: 8.941650 mA
     2123 driver.c 866: 12V_IN: 0.000000 V
     2126 main.c 74: POWER: Enabling all power rails
     2231 driver.c 864: VBAT: 3.629570 V
     2235 driver.c 865: IBAT: 15.797933 mA
     2239 driver.c 866: 12V_IN: 0.000000 V
     2243 sib3.c 151: SDCARD: Waiting for SD card
     2247 sib3.c 153: SDCARD: Card inserted
     2353 mmc.c 225: SDCARD: card initialized
     2357 sib3.c 171: SDCARD: Card initialization SUCCES; status: 0
     2376 sib3.c 705: SHT31 temperature: 24.511330 deg. C
     2381 sib3.c 706: SHT31 humidity: 45.876249 perc. RH
     3115 sib3.c 478: AD7708: CH1 zero scale call done
     3494 sib3.c 493: AD7708: CH1 full scale call done
     3600 sib3.c 508: AD7708: CH1 measurement done
     3605 sib3.c 556: AD7708: CH1 has value: 0.692901 V
     3610 sib3.c 134: THERMISTOR:  temperature = 24.139780
     3989 sib3.c 478: AD7708: CH2 zero scale call done
     4368 sib3.c 493: AD7708: CH2 full scale call done
     4474 sib3.c 508: AD7708: CH2 measurement done
     4479 sib3.c 556: AD7708: CH2 has value: 0.691221 V
     4484 sib3.c 134: THERMISTOR:  temperature = 24.224386
     4863 sib3.c 478: AD7708: CH3 zero scale call done
     5242 sib3.c 493: AD7708: CH3 full scale call done
     5348 sib3.c 508: AD7708: CH3 measurement done
     5353 sib3.c 556: AD7708: CH3 has value: 0.692003 V
     5358 sib3.c 134: THERMISTOR:  temperature = 24.185053
     5738 sib3.c 478: AD7708: CH4 zero scale call done
     6116 sib3.c 493: AD7708: CH4 full scale call done
     6222 sib3.c 508: AD7708: CH4 measurement done
     6227 sib3.c 556: AD7708: CH4 has value: 0.692120 V
     6233 sib3.c 134: THERMISTOR:  temperature = 24.179152
     6244 main.c 107: 1WIRE ROM: ff 02 84 19 00 00 (fcode 01)
     6250 sib3.c 600: RS232: Sending test string
```

```
38          <<< note: no data was received over RS-232 because
39              their was no loopback on the Rx and Tx lines. >>>
40      6357 sib3.c 629: RS485: Sending test string
41      6364 main.c 417: RSXXX data received: >>RS485 RS485 RS485 RS485
            RS485<<
42      6471 sib3.c 573: SDI12: Sending test string
43      6504 main.c 388: SD12 data received: >>SDI12 SDI12 SDI12 SDI12
            SDI12<<
44      6610 bolt.c 289: BOLT: send SUCESSFULL
45      6614 bolt.c 289: BOLT: send SUCESSFULL
46      6619 bolt.c 289: BOLT: send SUCESSFULL
47      6623 bolt.c 289: BOLT: send SUCESSFULL
```

Appendix C

Design Documents

This appendix provides an overview of all relevant design documents for the SIB3, and where to find them.

Design data can be found in two internal SVN repositories (only accessible for members of TIK).

The code for the `MSP432` can be found in the `https://svn.ee.ethz.ch/DualProcessorPlatform/code/application_processor/MSP432/sib3_test/` repository. All other design data can be found in the `https://svn.ee.ethz.ch/tecstuds/devaerep/` repository.

Important files and directories in the `/tecstuds/devaerep/` repository are:

altium/ contains the latest altium files.

board_shape/SIB_PCB_Board_2.dxf contains the board outline.

design_process_notes/SIB3_design_process_notes.tex contains notes about the design process of the SIB3. Some, but not all of these notes in this document are incorporated in this thesis.

DS/ contains datasheets of the various components in the design. It also contains relevant application notes.

BOM/ contains the bill of materials and order lists.

BOM/sib3_placement_BOM.xlsx provides a mapping between the reference designators and a `CMP NR`. All components in storage have their `CMP NR` marked on them, and are stored sorted on `CMP NR`.

papers/ contains some relevant papers.

rev1_design/ contains a snapshot of the design files for revision 1.

rev1_design/sib3_rev1.pdf is the schematic.

rev1_design/sib3_rev1_bottom_overlay.pdf is the bottom layer *printed circuit board* (PCB) overlay.

rev1_design/sib3_rev1_top_overlay.pdf is the top layer PCB overlay.

required_changes.txt lists everything that should be changed for a next board version.

rocketlogger/ contains power trace data recorded with the RocketLogger. Data files are named with a timestamp of the measurement, followed by the SVN commit number of the

code was active on the board. These commit numbers refer to the `DualProcessorPlatform` repository.

rocketlogger/plot_power_trace.m is a handy MATLAB script to plot the power traces recorded with the RocketLogger.

serial_out/ contains debug UART and BOLT outputs of the tests run on the board.

specification/functional_diagram.dia is the functional diagram of the SIB3.

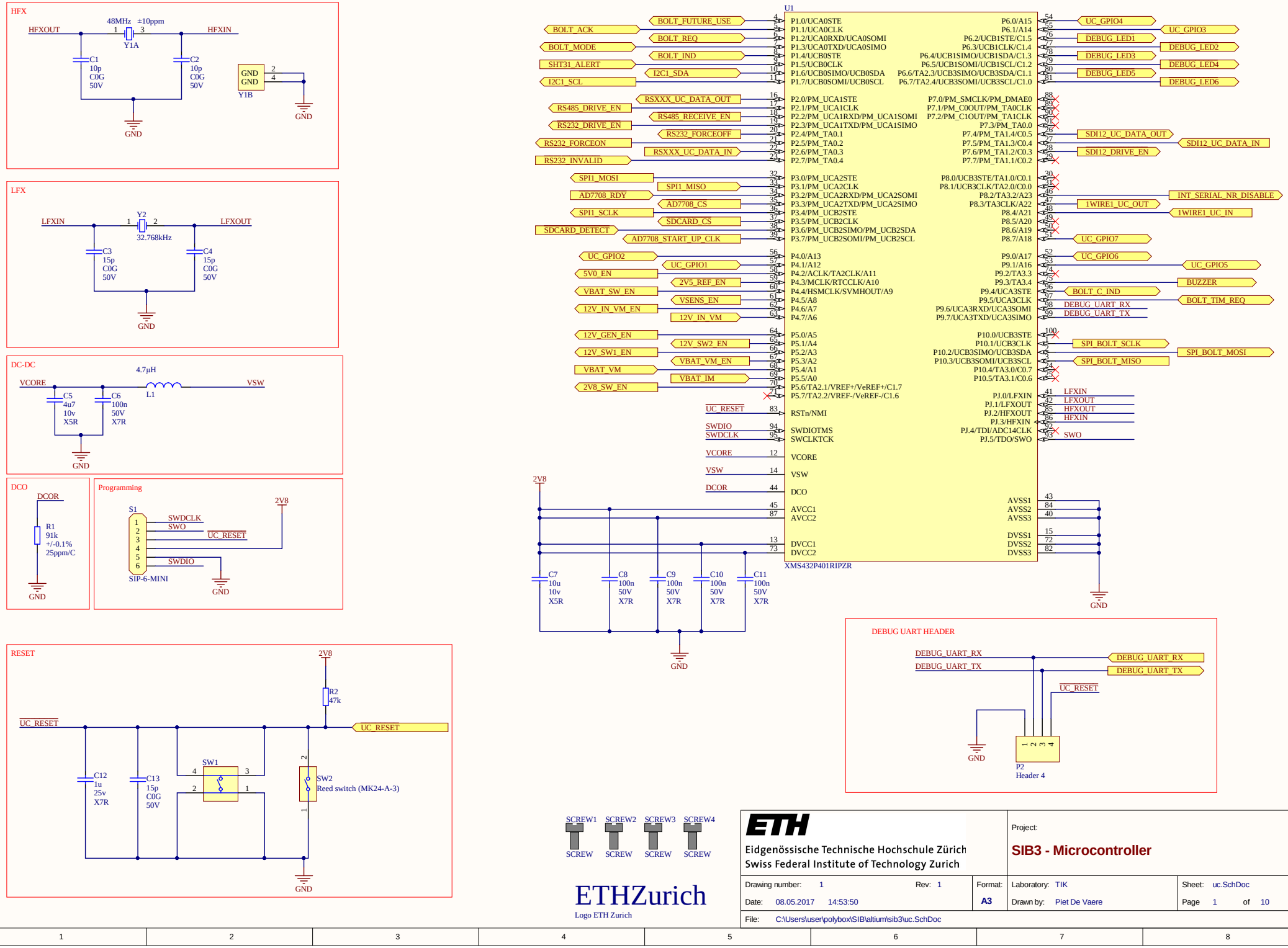
specification/power_concept.dia is the power diagram of the SIB3.

specification/URS_SIB3.doc is the specification document on which the SIB3 design is based.

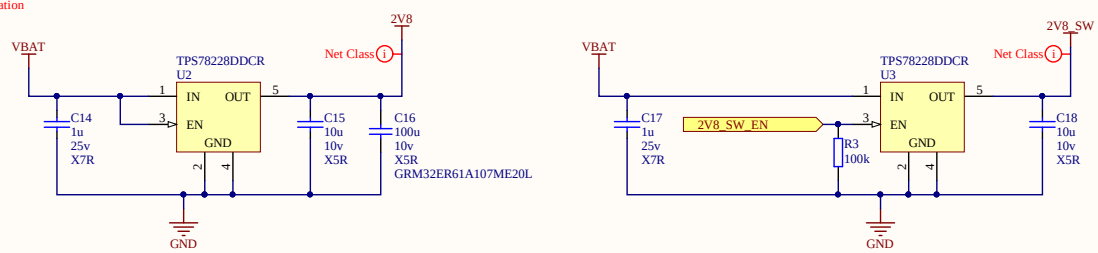
uc_pin_assignment/ contains the pin mapping of the `MSP432`. `.pinmux` files should be opened with the TI pinmux tool.

Appendix D

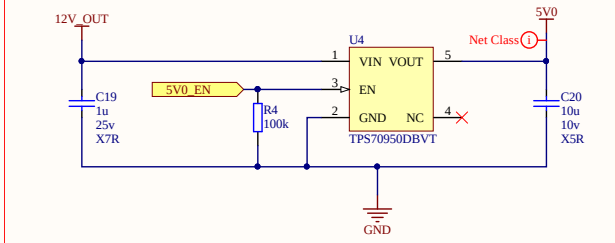
Schematic and PCB Overlay


HFX
48MHz ±10ppm
HFXOUT
HFXIN
Y1A
C1 10p C0G 50V
C2 10p C0G 50V
GND GND
Y1B
GND
GND
LFX
LFXIN
LFXOUT
Y2
32.768kHz
C3 15p C0G 50V
C4 15p C0G 50V
GND
DC-DC
4.7µH
VCORE
VSW
L1
C5 4u7 10v X5R
C6 100n 50V X7R
GND
DCO
DCOR
R1 91k +/-0.1% 25ppm/C
GND
Programming
2V8
S1
SWDCLK
SWO
UC_RESET
SWDIO
SIP-6-MINI
GND
RESET
2V8
R2 47k
UC_RESET
C12 1u 25v X7R
C13 15p C0G 50V
SW1
SW2
Reed switch (MK24-A-3)
GND
U1
P1.0/UCA0STE
P1.1/UCA0CLK
P1.2/UCA0RXD/UCA0SOMI
P1.3/UCA0TXD/UCA0SIMO
P1.4/UCB0STE
P1.5/UCB0CLK
P1.6/UCB0SIMO/UCB0SDA
P1.7/UCB0SOMI/UCB0SCL
P2.0/PM_UCA1STE
P2.1/PM_UCA1CLK
P2.2/PM_UCA1RXD/PM_UCA1SOMI
P2.3/PM_UCA1TXD/PM_UCA1SIMO
P2.4/PM_TA0.1
P2.5/PM_TA0.2
P2.6/PM_TA0.3
P2.7/PM_TA0.4
P3.0/PM_UCA2STE
P3.1/PM_UCA2CLK
P3.2/PM_UCA2RXD/PM_UCA2SOMI
P3.3/PM_UCA2TXD/PM_UCA2SIMO
P3.4/PM_UCB2STE
P3.5/PM_UCB2CLK
P3.6/PM_UCB2SIMO/PM_UCB2SDA
P3.7/PM_UCB2SOMI/PM_UCB2SCL
P4.0/A13
P4.1/A12
P4.2/ACLK/TA2CLK/A11
P4.3/MCLK/RTCCLK/A10
P4.4/HSMCLK/SVMHOUT/A9
P4.5/A8
P4.6/A7
P4.7/A6
P5.0/A5
P5.1/A4
P5.2/A3
P5.3/A2
P5.4/A1
P5.5/A0
P5.6/TA2.1/VREF+/VeREF+/C1.7
P5.7/TA2.2/VREF-/VeREF-/C1.6
RSTn/NMI
SWDIOTMS
SWCLKTCK
VCORE
VSW
DCO
AVCC1
AVCC2
DVCC1
DVCC2
P6.0/A15
P6.1/A14
P6.2/UCB1STE/C1.5
P6.3/UCB1CLK/C1.4
P6.4/UCB1SIMO/UCB1SDA/C1.3
P6.5/UCB1SOMI/UCB1SCL/C1.2
P6.6/TA2.3/UCB3SIMO/UCB3SDA/C1.1
P6.7/TA2.4/UCB3SOMI/UCB3SCL/C1.0
P7.0/PM_SMCLK/PM_DMAE0
P7.1/PM_C0OUT/PM_TA0CLK
P7.2/PM_C1OUT/PM_TA1CLK
P7.3/PM_TA0.0
P7.4/PM_TA1.4/C0.5
P7.5/PM_TA1.3/C0.4
P7.6/PM_TA1.2/C0.3
P7.7/PM_TA1.1/C0.2
P8.0/UCB3STE/TA1.0/C0.1
P8.1/UCB3CLK/TA2.0/C0.0
P8.2/TA3.2/A23
P8.3/TA3CLK/A22
P8.4/A21
P8.5/A20
P8.6/A19
P8.7/A18
P9.0/A17
P9.1/A16
P9.2/TA3.3
P9.3/TA3.4
P9.4/UCA3STE
P9.5/UCA3CLK
P9.6/UCA3RXD/UCA3SOMI
P9.7/UCA3TXD/UCA3SIMO
P10.0/UCB3STE
P10.1/UCB3CLK
P10.2/UCB3SIMO/UCB3SDA
P10.3/UCB3SOMI/UCB3SCL
P10.4/TA3.0/C0.7
P10.5/TA3.1/C0.6
PJ.0/LFXIN
PJ.1/LFXOUT
PJ.2/HFXOUT
PJ.3/HFXIN
PJ.4/TDI/ADC14CLK
PJ.5/TDO/SWO
AVSS1
AVSS2
AVSS3
DVSS1
DVSS2
DVSS3
XMS432P401RIPZR
BOLT_FUTURE_USE
BOLT_ACK
BOLT_REQ
BOLT_MODE
BOLT_IND
SHT31_ALERT
I2C1_SDA
I2C1_SCL
RSXXX_UC_DATA_OUT
RS485_DRIVE_EN
RS485_RECEIVE_EN
RS232_DRIVE_EN
RS232_FORCEOFF
RS232_FORCEON
RSXXX_UC_DATA_IN
RS232_INVALID
SPI1_MOSI
SPI1_MISO
AD7708_RDY
AD7708_CS
SPI1_SCLK
SDCARD_CS
SDCARD_DETECT
AD7708_START_UP_CLK
UC_GPIO2
UC_GPIO1
5V0_EN
2V5_REF_EN
VBAT_SW_EN
VSENS_EN
12V_IN_VM_EN
12V_IN_VM
12V_GEN_EN
12V_SW2_EN
12V_SW1_EN
VBAT_VM_EN
VBAT_VM
VBAT_IM
2V8_SW_EN
UC_RESET
SWDIO
SWDCLK
VCORE
VSW
DCOR
2V8
C7 10u 10v X5R
C8 100n 50V X7R
C9 100n 50V X7R
C10 100n 50V X7R
C11 100n 50V X7R
GND
UC_GPIO4
UC_GPIO3
DEBUG_LED1
DEBUG_LED2
DEBUG_LED3
DEBUG_LED4
DEBUG_LED5
DEBUG_LED6
SDI12_UC_DATA_OUT
SDI12_UC_DATA_IN
SDI12_DRIVE_EN
INT_SERIAL_NR_DISABLE
1WIRE1_UC_OUT
1WIRE1_UC_IN
UC_GPIO7
UC_GPIO6
UC_GPIO5
BUZZER
BOLT_C_IND
BOLT_TIM_REQ
DEBUG_UART_RX
DEBUG_UART_TX
SPI_BOLT_SCLK
SPI_BOLT_MOSI
SPI_BOLT_MISO
LFXIN
LFXOUT
HFXOUT
HFXIN
SWO
GND
DEBUG UART HEADER
DEBUG_UART_RX
DEBUG_UART_TX
UC_RESET
GND
P2
Header 4
SCREW1
SCREW2
SCREW3
SCREW4
SCREW
ETHZurich
Logo ETH Zurich
Eidgenössische Technische Hochschule Zürich
Swiss Federal Institute of Technology Zurich
Project:
SIB3 - Microcontroller
Drawing number: 1
Rev: 1
Format: A3
Laboratory: TIK
Sheet: uc.SchDoc
Date: 08.05.2017 14:53:50
Drawn by: Piet De Vaere
Page 1 of 10
File: C:\Users\user\polybox\SIB\altium\sib3\uc.SchDoc

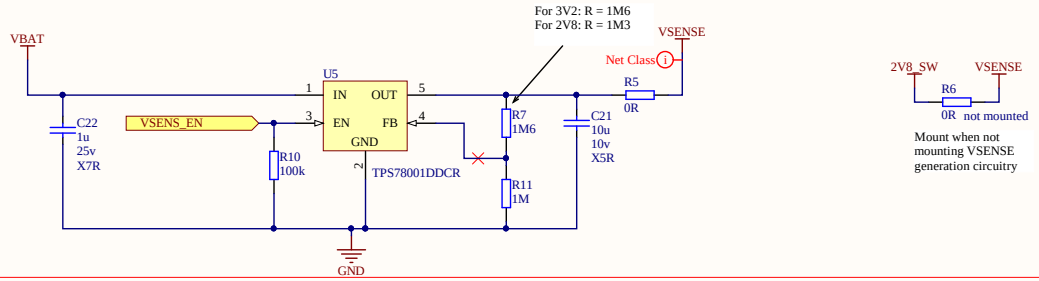
2V8 generation



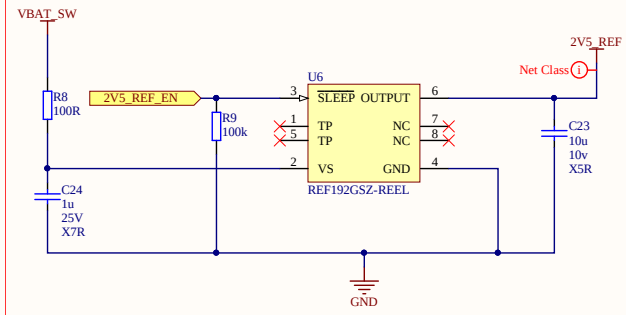
5V0 generation



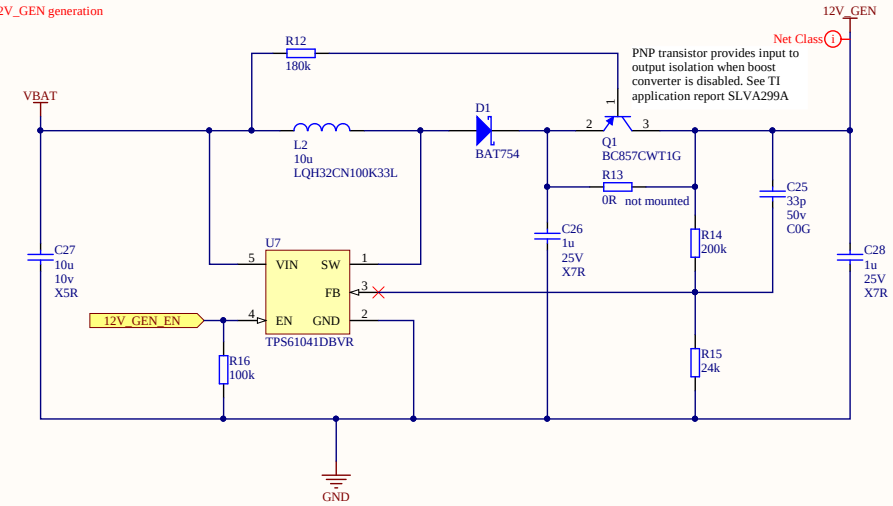
VSENSE generation



2V5 reference generation



12V_GEN generation



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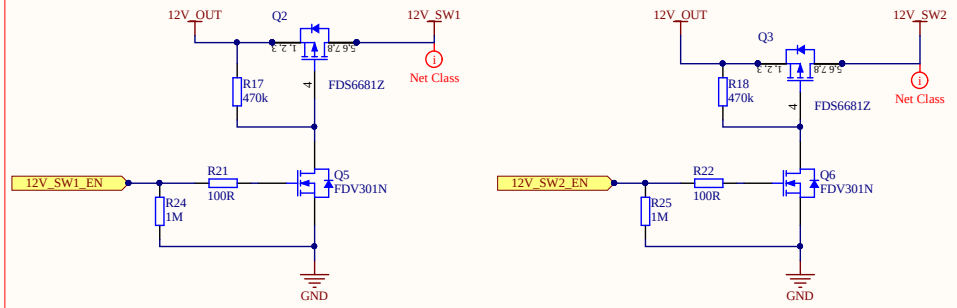
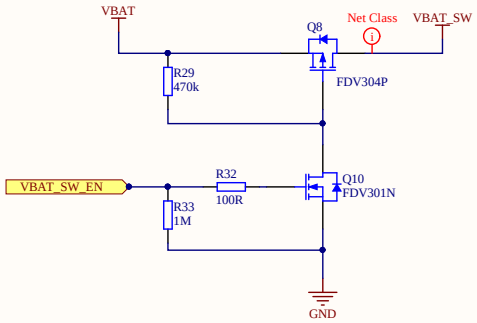
Date: 08.05.2017 14:53:50				Drawn by: Piet De Vaere	Page 2 of 10
File: C:\Users\user\polybox\SIB\altium\sib3\power_generation.SchDoc					

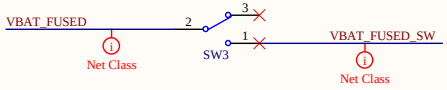
12V switching



VBAT switching

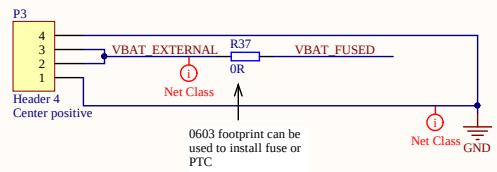


Main power switch

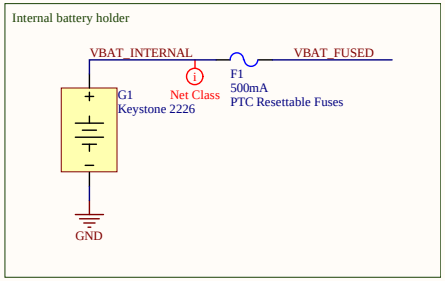


Battery connectors

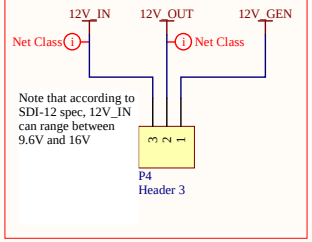
Terminal for external power supply



Internal battery holder

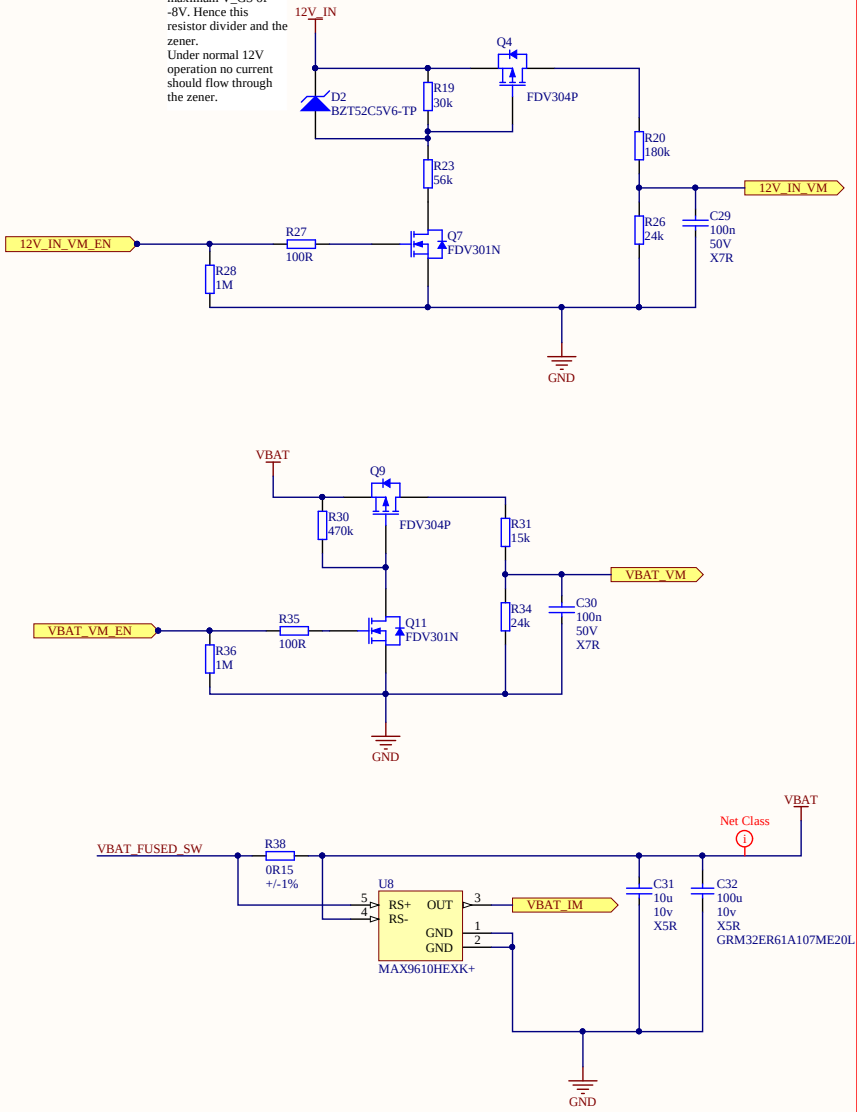


12V selection



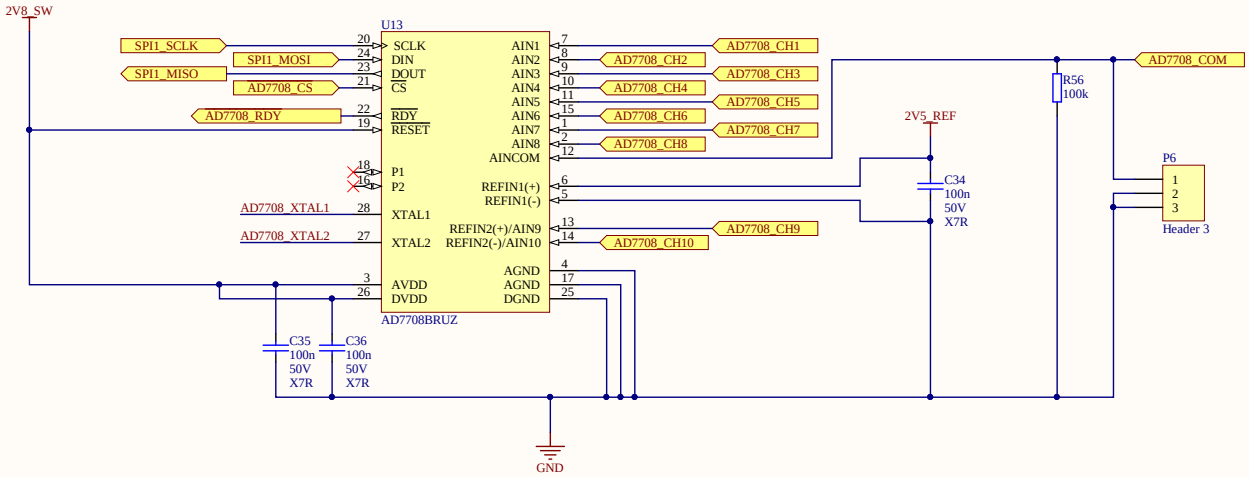
Voltage and Current monitors

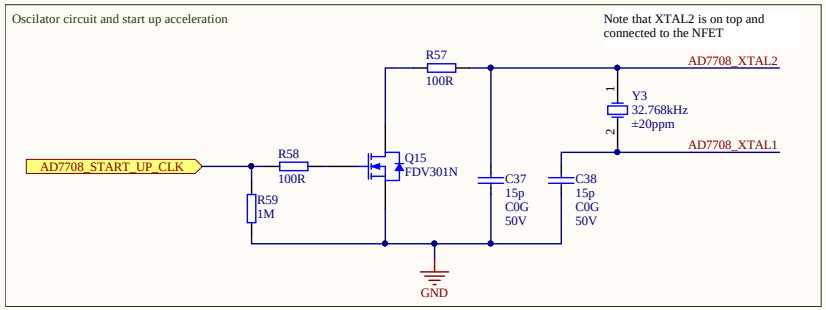
The FDV304P has a maximum V_GS of -8V. Hence this resistor divider and the zener.
Under normal 12V operation no current should flow through the zener.



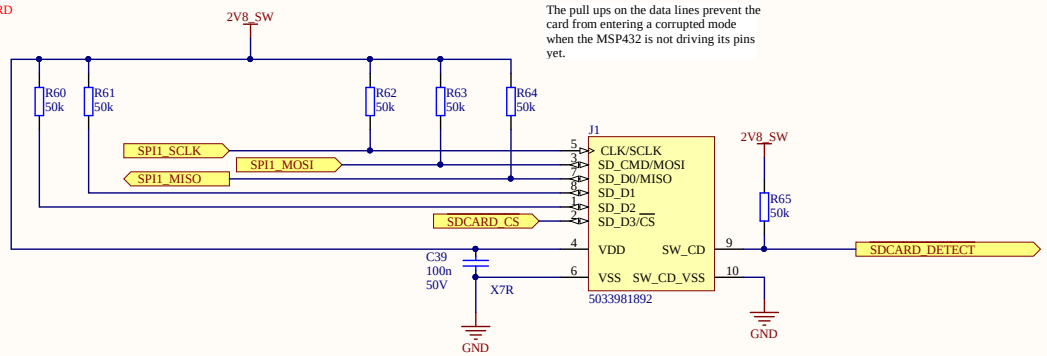
ETH Eidgenössische Technische Hochschule Zürich Swiss Federal Institute of Technology Zurich				Project: SIB3 - Power switching	
Drawing number: 3	Rev: 1	Format: A3		Laboratory: TIK	Sheet: power_switching.SchDoc
Date: 08.05.2017 14:53:50				Drawn by: Piet De Vaere	Page 3 of 10
File: C:\Users\user\polybox\SIB\altium\sib3\power_switching.SchDoc					

Precision external ADC



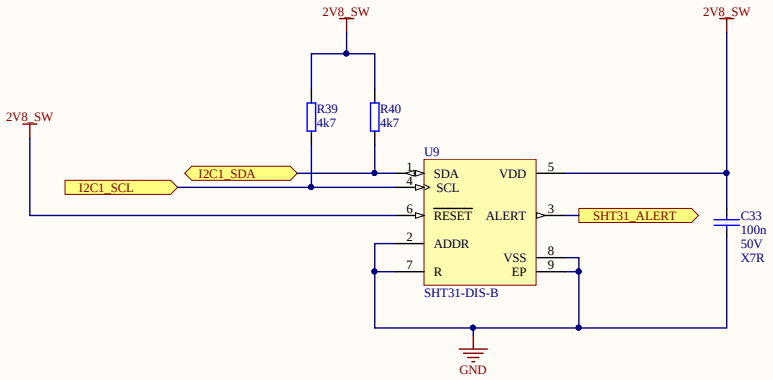


SDCARD

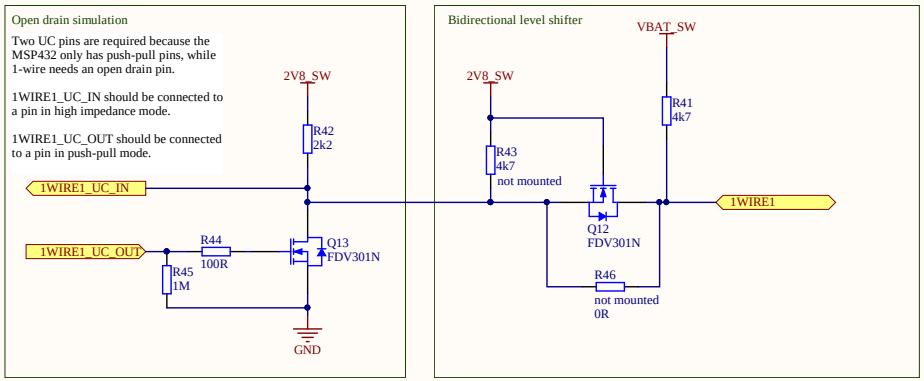


ETH Eidgenössische Technische Hochschule Zürich Swiss Federal Institute of Technology Zurich			Project: SIB3 - SPI: ADC and SD card	
Drawing number: 4	Rev: 1	Format: A3	Laboratory: TIK	Sheet: spi.SchDoc
Date: 08.05.2017 14:53:50			Drawn by: Piet De Vaere	Page 4 of 10
File: C:\Users\user\polybox\SIB\altium\sib3\spi.SchDoc				

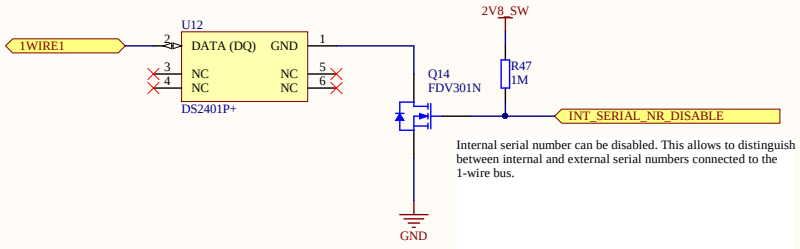
Sensirion humidity and temperature sensor



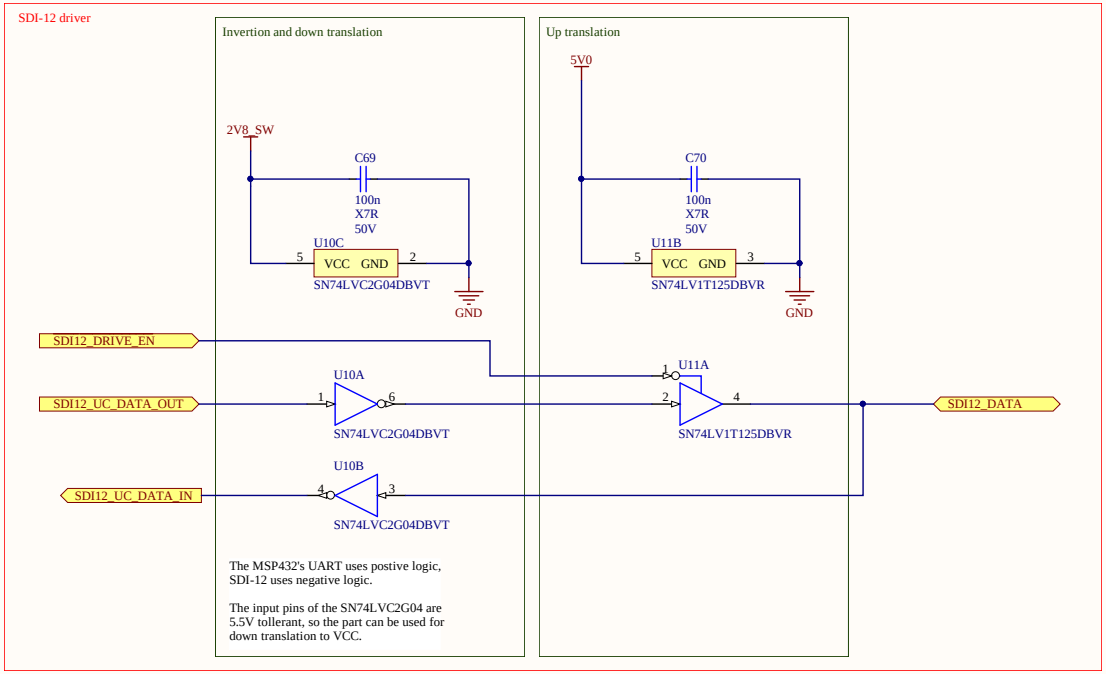
1-wire driver



Internal silicon serial number



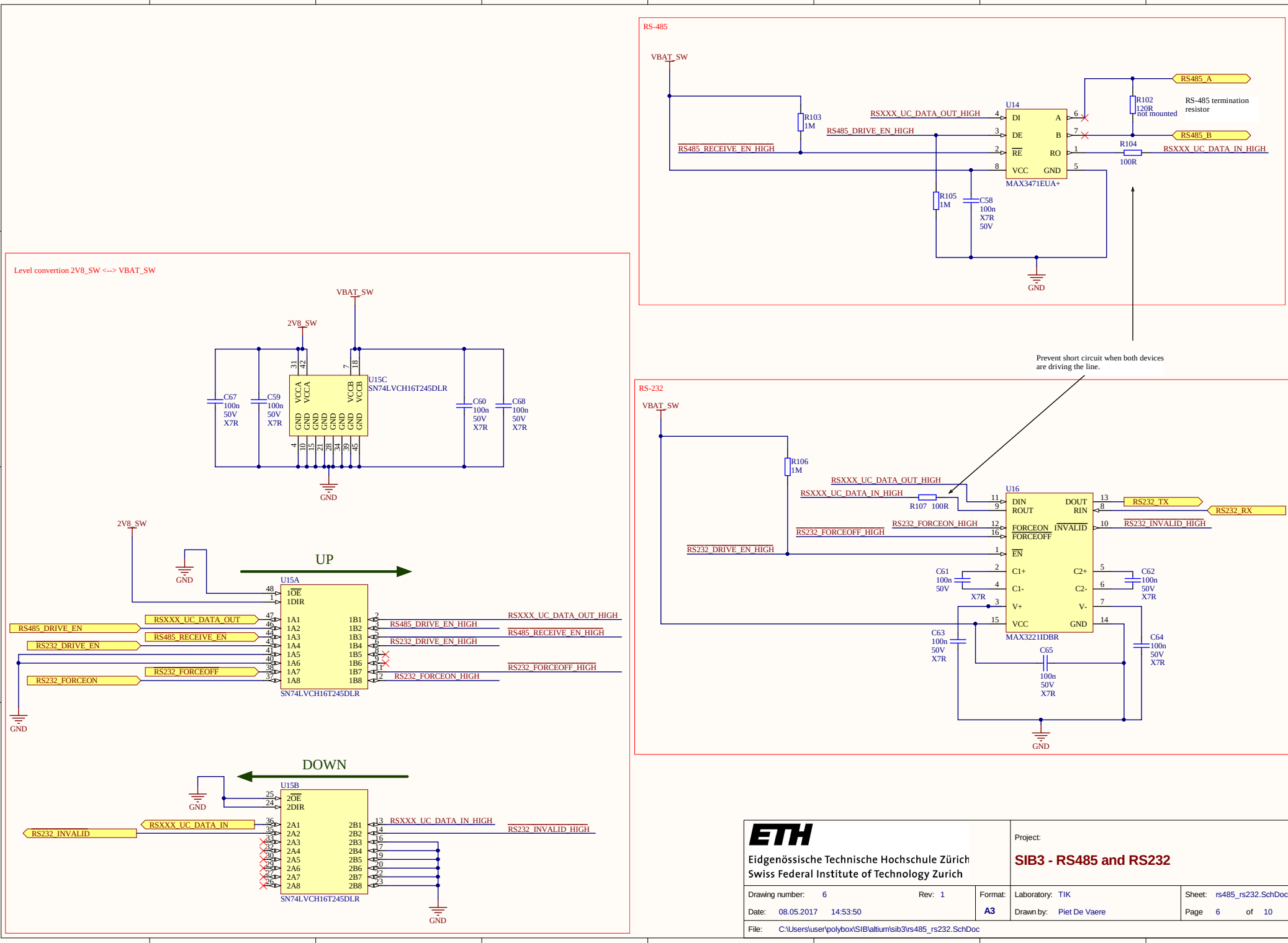
SDI-12 driver



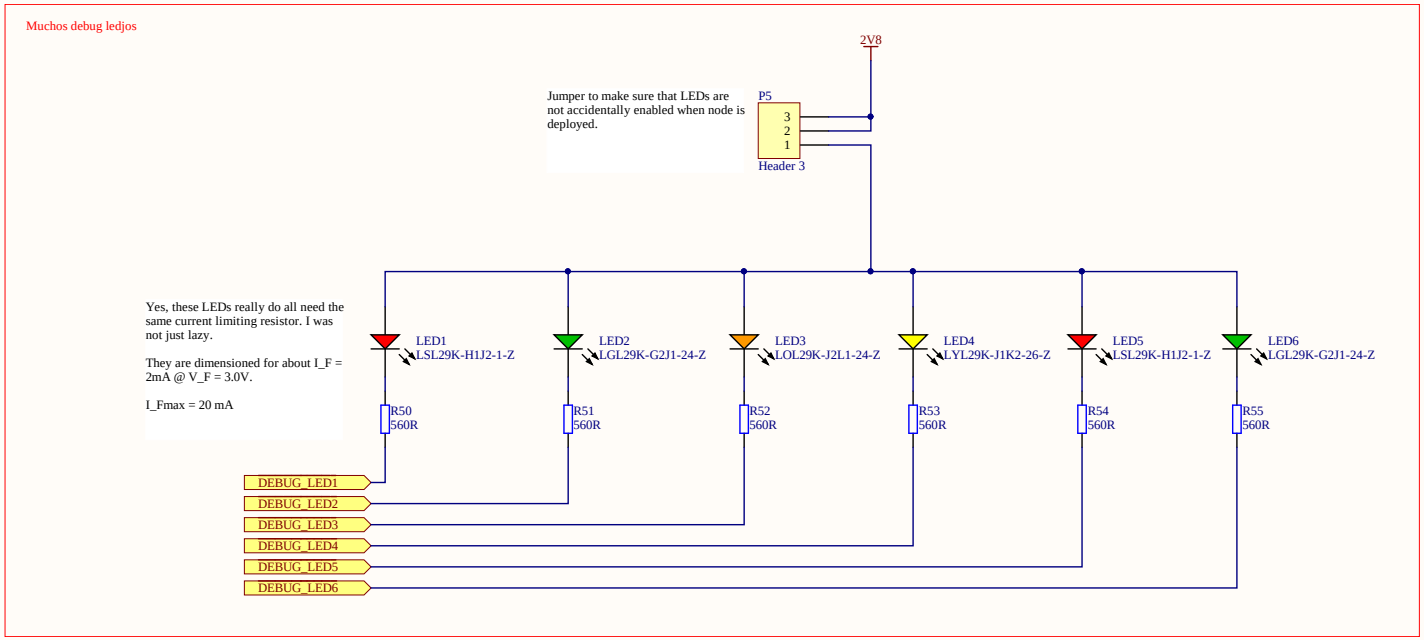
Eidgenössische Technische Hochschule Zürich
Swiss Federal Institute of Technology Zurich

Project: **SIB3 - I2C1, 1WIRE1, SDI12**

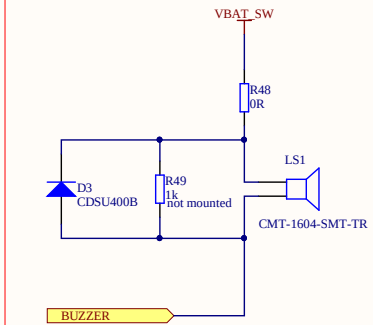
Drawing number: 5	Rev: 1	Format: A3	Laboratory: TIK	Sheet: i2c1_1wire1_sdi12.SchDoc	
Date: 08.05.2017 14:53:50			Drawn by: Piet De Vaere	Page 5	of 10
File: C:\Users\user\polybox\SIB\altium\sib3\i2c1_1wire1_sdi12.SchDoc					


RS-485
VBAT_SW
R103
1M
RSXXX_UC_DATA_OUT_HIGH
RS485_DRIVE_EN_HIGH
RS485_RECEIVE_EN_HIGH
U14
DI
DE
RE
VCC
A
B
RO
GND
MAX3471EUA+
RS485_A
RS485_B
R102
120R
not mounted
RS-485 termination resistor
R104
100R
RSXXX_UC_DATA_IN_HIGH
R105
1M
C58
100n
X7R
50V
GND
Level convertion 2V8_SW <--> VBAT_SW
VBAT_SW
2V8_SW
C67
100n
50V
X7R
C59
100n
50V
X7R
U15C
SN74LVCH16T245DLR
VCCA
VCCB
GND
C60
100n
50V
X7R
C68
100n
50V
X7R
GND
2V8_SW
GND
UP
U15A
1OE
1DIR
1A1
1A2
1A3
1A4
1A5
1A6
1A7
1A8
1B1
1B2
1B3
1B4
1B5
1B6
1B7
1B8
RSXXX_UC_DATA_OUT
RS485_DRIVE_EN
RS485_RECEIVE_EN
RS232_DRIVE_EN
RS232_FORCEOFF
RS232_FORCEON
RS485_DRIVE_EN_HIGH
RS232_DRIVE_EN_HIGH
RS232_FORCEON_HIGH
RSXXX_UC_DATA_OUT_HIGH
RS485_RECEIVE_EN_HIGH
RS232_FORCEOFF_HIGH
SN74LVCH16T245DLR
GND
DOWN
U15B
2OE
2DIR
2A1
2A2
2A3
2A4
2A5
2A6
2A7
2A8
2B1
2B2
2B3
2B4
2B5
2B6
2B7
2B8
RSXXX_UC_DATA_IN
RS232_INVALID
RSXXX_UC_DATA_IN_HIGH
RS232_INVALID_HIGH
SN74LVCH16T245DLR
GND
Prevent short circuit when both devices are driving the line.
RS-232
VBAT_SW
R106
1M
RSXXX_UC_DATA_OUT_HIGH
RSXXX_UC_DATA_IN_HIGH
R107 100R
RS232_FORCEOFF_HIGH
RS232_FORCEON_HIGH
RS232_DRIVE_EN_HIGH
U16
DIN
ROUT
FORCEON
FORCEOFF
EN
C1+
C1-
V+
VCC
DOUT
RIN
INVALID
C2+
C2-
V-
GND
MAX3221IDBR
RS232_TX
RS232_RX
RS232_INVALID_HIGH
C61
100n
50V
X7R
C62
100n
50V
X7R
C63
100n
50V
X7R
C64
100n
50V
X7R
C65
100n
50V
X7R
GND
ETH
Eidgenössische Technische Hochschule Zürich
Swiss Federal Institute of Technology Zurich
Project:
SIB3 - RS485 and RS232
Drawing number: 6
Rev: 1
Format: A3
Laboratory: TIK
Sheet: rs485_rs232.SchDoc
Date: 08.05.2017 14:53:50
Drawn by: Piet De Vaere
Page 6 of 10
File: C:\Users\user\polybox\SIB\altium\sib3\rs485_rs232.SchDoc

Muchos debug ledjos

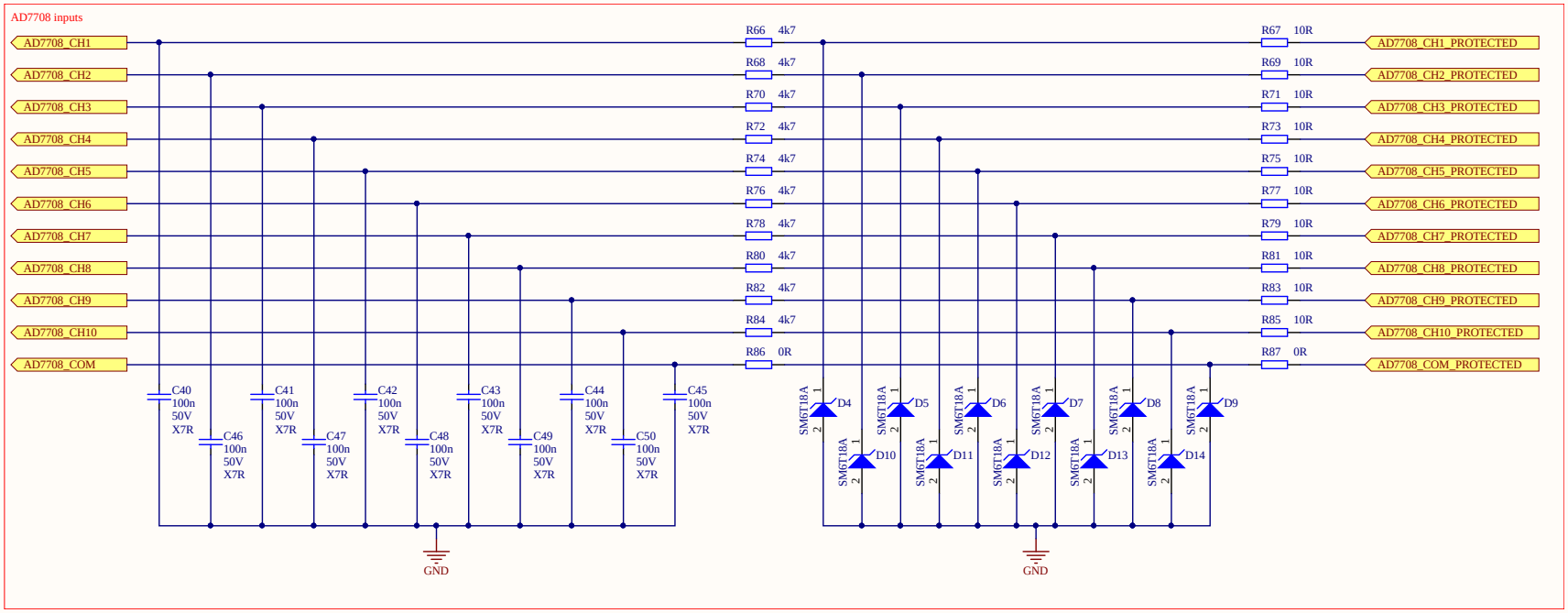


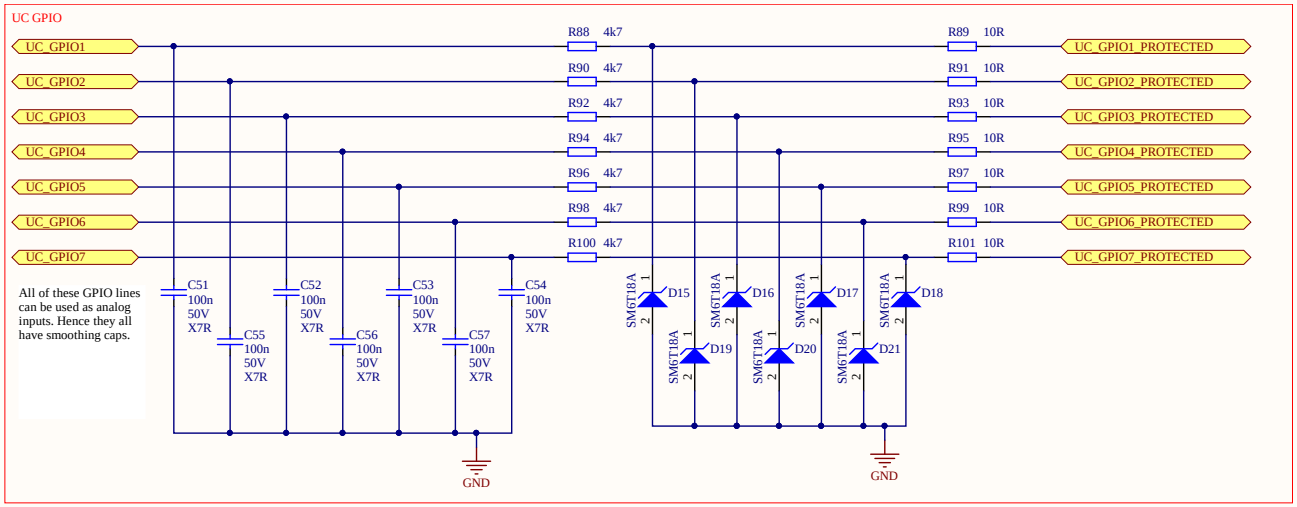
Buzzer



Eidgenössische Technische Hochschule Zürich Swiss Federal Institute of Technology Zurich			Project: SIB3 - LEDs and buzzer	
Drawing number: 7 Rev: 1 Date: 08.05.2017 14:53:50	Format: A3	Laboratory: TIK Drawn by: Piet De Vaere	Sheet: leds_buzzer.SchDoc Page 7 of 10	
File: C:\Users\user\polybox\SIB\altium\sib3\leds_buzzer.SchDoc				

!!RED!!





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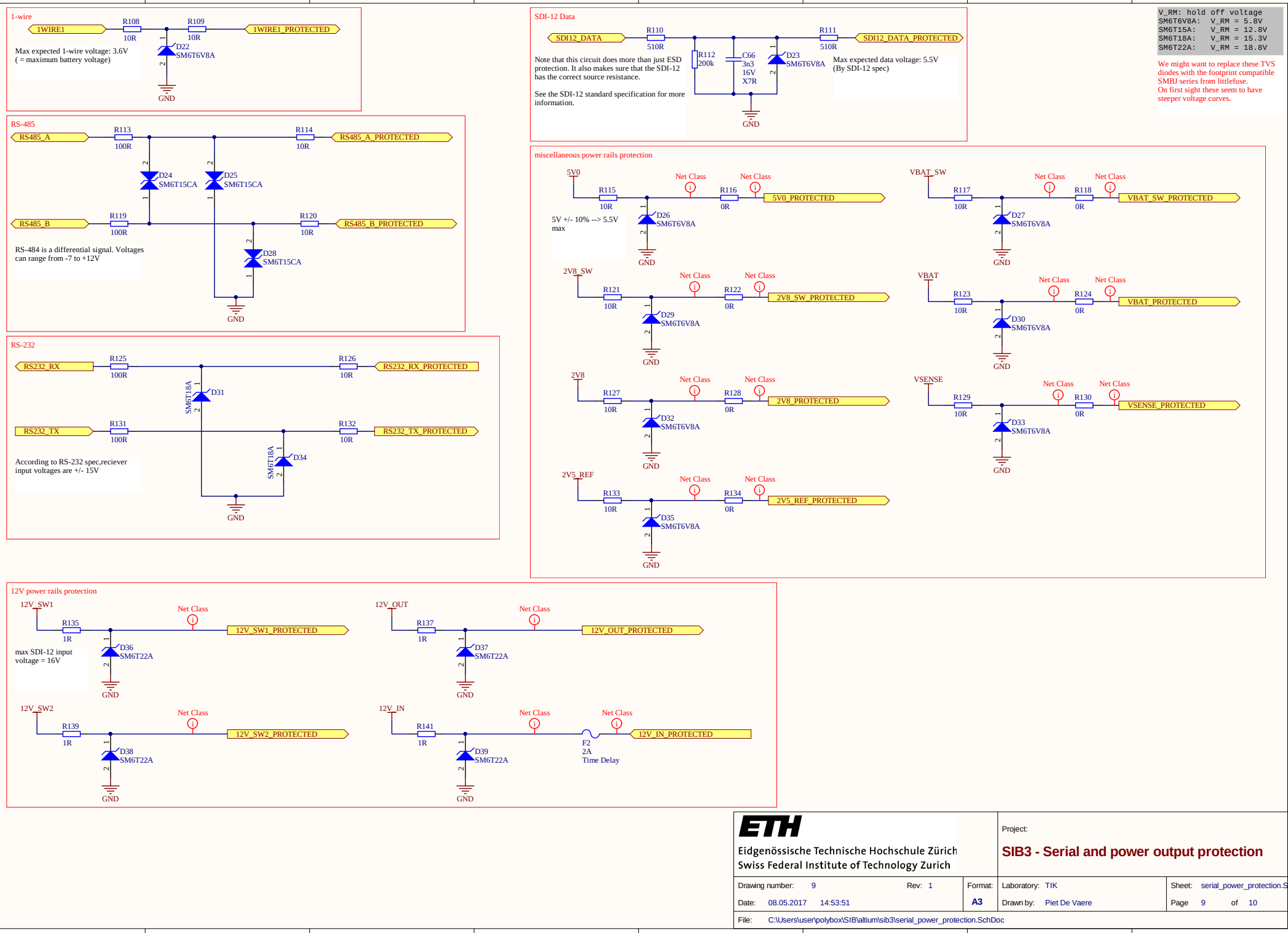
Project:

SIB3 - ADC and GPIO output protection

Drawing number: 8	Rev: 1	Format: A3	Laboratory: TIK	Sheet: adc_gpio_protection.SchDoc	
Date: 08.05.2017 14:53:51			Drawn by: Piet De Vaere	Page 8 of 10	
File: C:\Users\user\polybox\SIB\altium\sib3\adc_gpio_protection.SchDoc					



ETH

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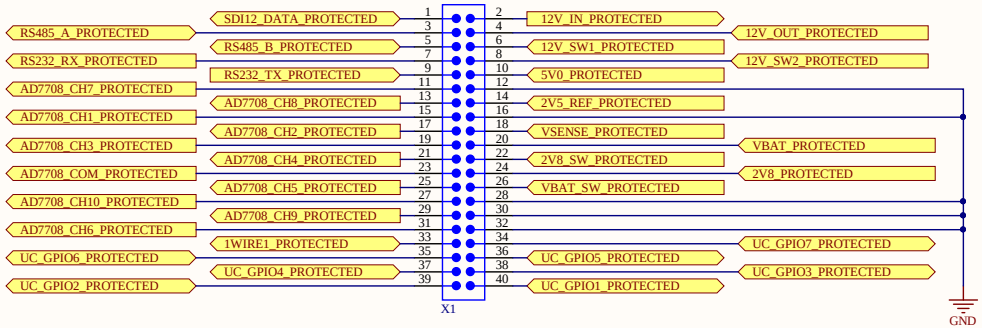
Project:

SIB3 - Serial and power output protection

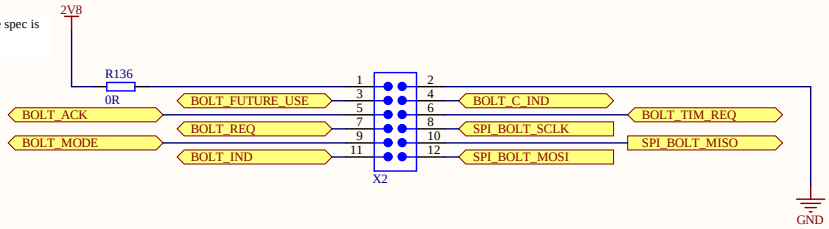
Drawing number: 9	Rev: 1	Format: A3	Laboratory: TIK	Sheet: serial_power_protection.SchDoc	
Date: 08.05.2017 14:53:51			Drawn by: Piet De Vaere	Page 9 of 10	
File: C:\Users\user\polybox\SIB\altium\sib3\serial_power_protection.SchDoc					

Main Harting connector. Connects to Souriau plug.



BOLT header

Header to be replaced and repinned once spec is received



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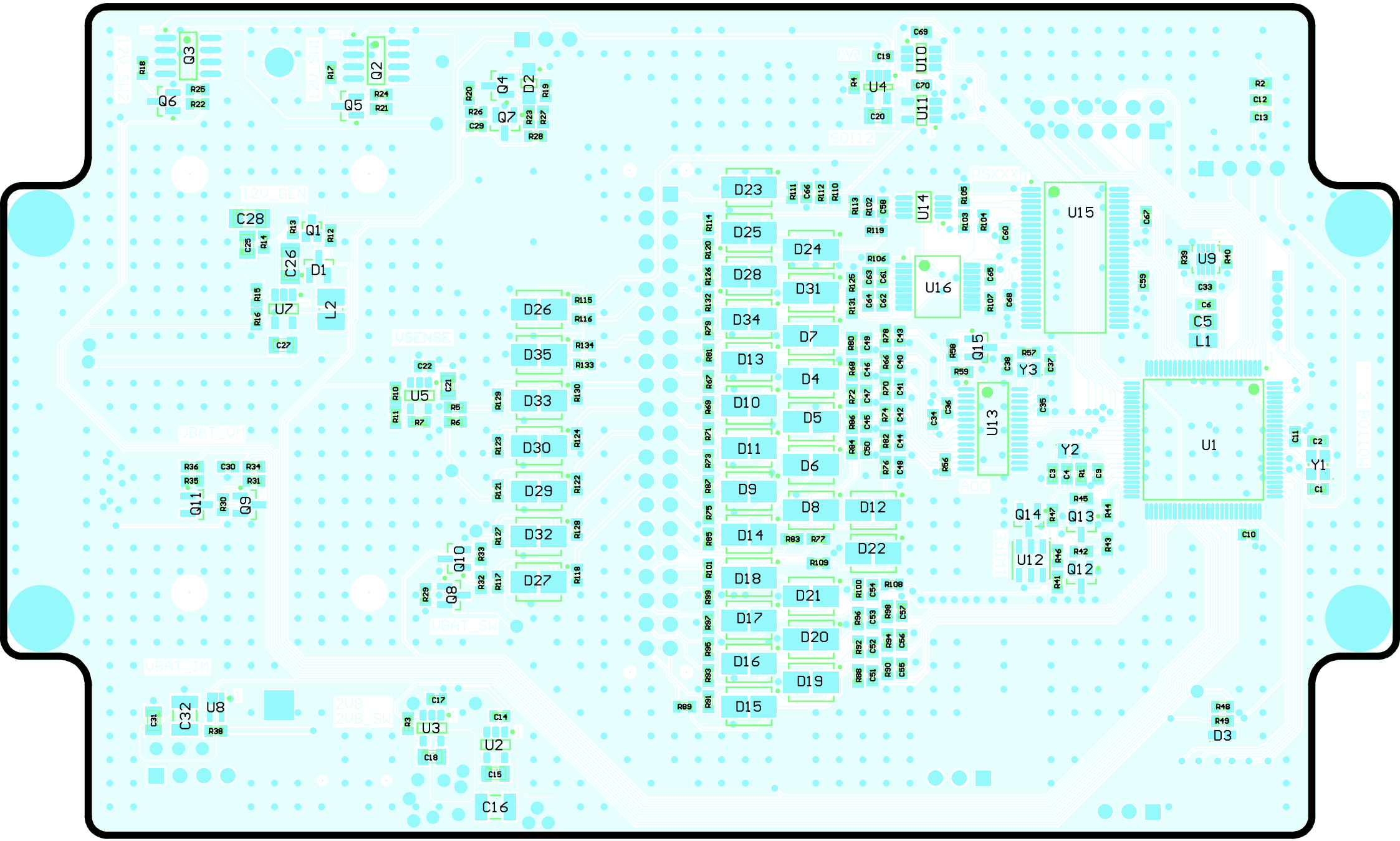
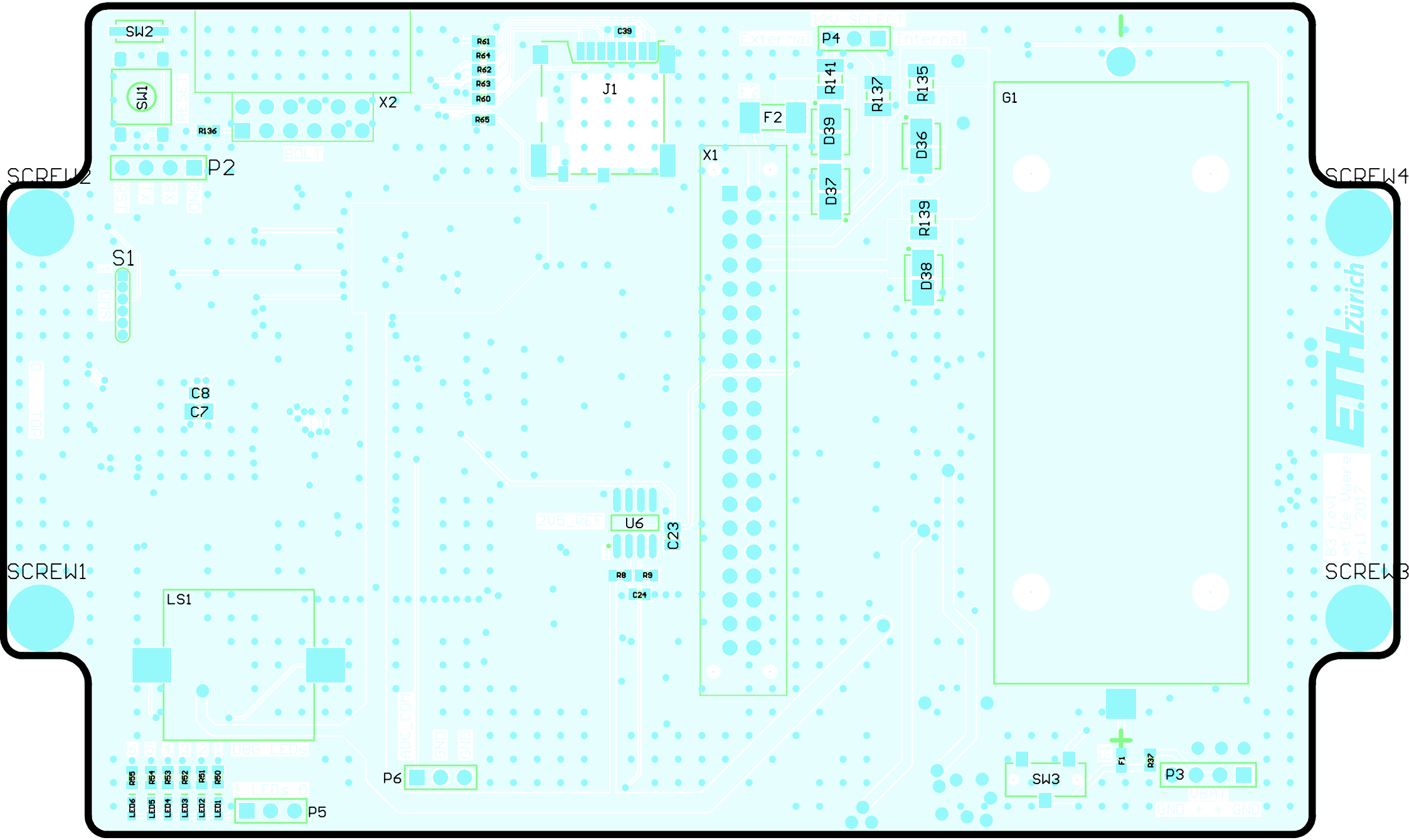
Project: **SIB3 - Connectors**

Drawing number: 10	Rev: 1	Format: A3	Laboratory: TIK	Sheet: connectors.SchDoc	
Date: 08.05.2017 14:53:51			Drawn by: Piet De Vaere	Page 10 of 10	
File: C:\Users\user\polybox\SIB\altium\sib3\connectors.SchDoc					

CAMtasticDXP (TM):



CAMtasticDXP (TM):